B 249

DATA TRANSMISSION CONTROL UNIT

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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FUNCTIONAL DETAIL

CIRCUIT DETAIL

ADJUSTMENTS

MAINTENANCE PROCEDURES

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RELIABILITY IMPROVEMENT NOTICES

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MODIFICATIONS (BRANCH LIBRARIES)

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Introduction & Operation

B249 DATA TRANSMISSION CONTROL UNIT - GENERAL DESCRIPTION

The B249 DTCU is required when:

1. More than one B487 DTTU is used on a single Processing System.
2. Intermixing existing Terminal Units with the B487 DTTU (B481, B483, B484 & B486).
3. Code translation from the character representation of the Remote device to that used by the Processing System is to be accomplished Hardware-wise rather than Programmatically.

Up to 15 B487 Data Transmission Terminal Units can be accommodated on a B5500 through the B249 Data Transmission Control Unit. The maximum number of B487 DTTUs on a B300 is four. Refer to Figure I-1.

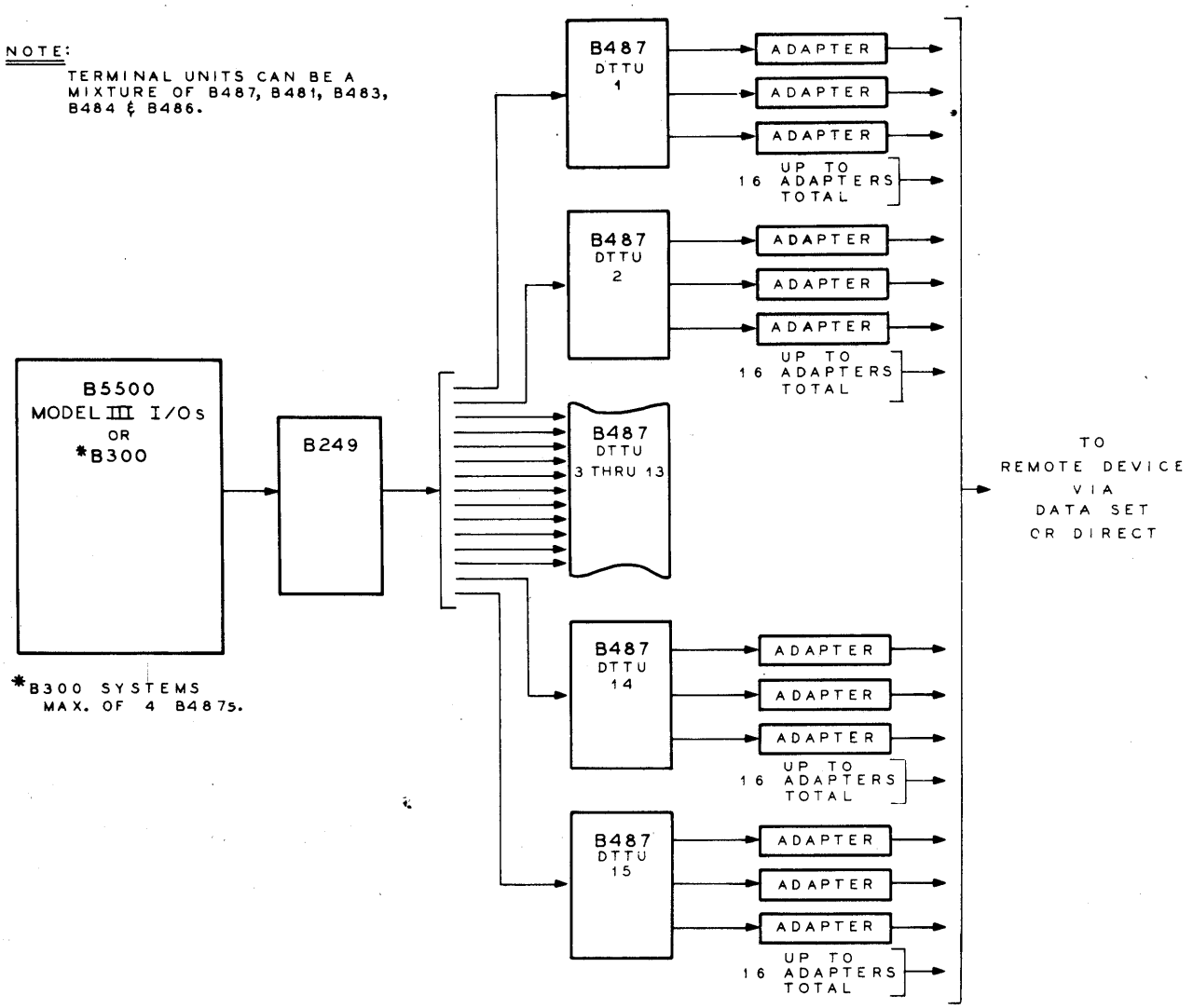


FIGURE I-1
DATA COMMUNICATIONS CONFIGURATION

Introduction & Operation

All presently existing Data Communication Terminal Units can be connected to the B300 or B5500 through the B249 DTCU, either singularly or in combination with B487 DTTUs. Specifically, the following Terminal Units can be attached to a B249 DTCU.

B487 Data Transmission Terminal Unit

B481 Teletype Terminal Unit
B483 Typewriter Terminal Unit
B484 TWX Terminal Unit
B486 Central Terminal Unit
} Inquiry Type Terminals

When intermixing Inquiry Terminal Units with the B487 DTTUs on the B300, the maximum number of B487s is three (3), while accomodating up to 12 Inquiry Terminals. Up to 15 Terminal Units, independent of type, can be handled on a B5500.

Because the Code Translator which translates BCL to ASCII or Baudot and vice versa is contained in the B249 DTCU, the code translation must be accomplished Programmatically when the B249 DTCU is not used.

The Transfer and Translate Command of the B300 aids in the programmatic translation of codes, but the fastest and most efficient method to provide this translation is by means of the B249 Data Transmission Control Unit.

The B249 DTCU occupies one standard rack or gate and can be mounted in the A Rack or E Rack position of a B450 or B452 Cabinet.

Any exchange of information between the Processing System and a Remote device (or vice versa) is routed through the DTCU.

The DTCU notifies the Processing System whenever a DTTU is in an Interrupt State by Scanning until that DTTU which contains an Interrupt is located. When the Processing System responds to the Interrupt with a Passive Interrogate, the DTCU supplies the Terminal Unit number to the System and initiates a DTTU Cycle which informs the Processing System as to the Status and Number of the Buffer being Interrogated.

During System Activity (Read/Write), the DTCU acts as a Buffer and Translator between the DTTU and the Processing System.

During a Read operation, the DTCU accepts a character at a time from the System, translates to the ASCII or Baudot and relays the character to the DTTU where it is stored in Buffer Memory.

When communicating with a Buffer serviced by an Adapter that is receiving BCL code, the Translator is by-passed.

PHYSICAL DESCRIPTION

The DTCU (B249) occupies the A and B Panels of one gate (see Figure I-2).

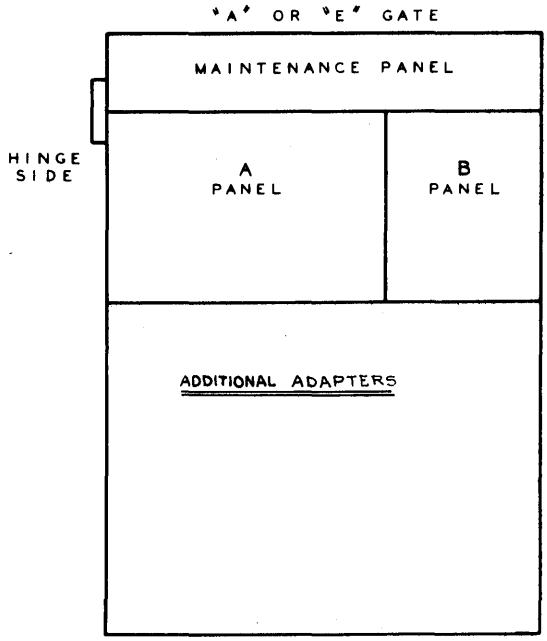


FIGURE I-2
DTCU PANEL LAYOUT

A maximum of one (1) DTCU can be used with the B300/B5500 System.

The DTCU can be mounted on either the A or E Rack positions of a B450 or B452 (B5500 type) Cabinet. Power consumption and heat dissipation per DTCU are as follows:

BTU - 250
KVA - .075

GLOSSARY - DTCU & SYSTEM

ABCL-SYS - Abnormal Condition Level

Sent to Processor during the Sync Operation of a Read or Write Command. Used only with the B300 Processor.

B5KL - B5500 Identification Level

When true, indicates DTC is connected to a B5500 System. This line is ground when DTC is connected to a B300 Processor.

NOTE

The term B5KL in the DTC is SIDL (System Identification Level) at the Processor end of the cable.

IFAL-SYS - Inquiry Final Address

When true, informs the Processing System that the Final

Address location of the designated Buffer is addressed.

INnL-SYS - Information Bits To System

When true, an INnL (n = 1, 2, 4, 8, A, B) signal denotes a 1-bit in the corresponding position of a Character Code is sent to the System.

IRRL-SYS - Inquiry Read-Ready Level

When true, the Buffer Control word of the designated Adapter indicates Read-Ready.

ISRL/-SYS - Inquiry System Ready Level

When false, indicates that the DTC is Ready. Power ON, Remote State.

ISYL/ - Initiate Sync Operation

When False, ISYL/ signifies that the System is beginning the execution of a Data Communication Instruction.

ITCL/-SYS - Inquiry Time for Character

When false, indicates that the DTC has received or is ready to transfer an individual character to the Processing System.

IWRL-SYS - Inquiry Write-Ready Level

When true, the Buffer Control word of the designated Adapter indicates Write-Ready.

MV8L - B300 M-Variant, 8-Bit

When true, indicates that the M-Variant 8-bit in the B300 is a "1". This condition indicates the following:

Interrogate Order - Buffer number on the OInL/ lines are significant.

Read or Write Order - Ignore Group Mark code during Information Transfer. Buffer number on the OInL/ lines are significant.

OInL/ - Output Information Bits

When false, an OInL (n = 1, 2, 4, 8, A, B) signal denotes a 1-bit in the corresponding position of a Character Code sent from the System.

RINL/ - Read Information Level

When false, signifies that the Processing System is performing a Read Operation.

SCAL/-SYS - Scan In Progress - B300 Only

When false, indicates the DTC is performing internal oper-

ations and is unable to react to a false ISYL/ signal. When this condition exists, the B300 will hold the execution of the Interrogate Command.

SIIL/-SYS - Set Interrupt Level

When false, indicates that a Buffer requires attention of the Processing System.

TUBL-SYS - Terminal Unit/Adapter Busy Level

When true, indicates the designated Adapter is in a Busy State consisting of:

1. The Buffer Control Word Busy bit (DA2F) is ON.

or

2. The Buffer Control Word indicates the Buffer is In Use by the Adapter, DB6F ON.

TURL/-SYS - Terminal/Adapter Ready Level

When false, indicates the following:

1. The Terminal Unit is Ready. Power ON, Remote State.
2. An Adapter is connected to the addressed Buffer and the Not-Ready bit of the Buffer Control Word is OFF.

WIRL/ - Write Information Level

When false, signifies that the Processing System is performing a Write Operation.

GLOSSARY - DATA TRANSMISSION TERMINAL UNIT & DTCU

DTTL/-DTT - Data Transmission Terminal Level

This level is false when the DTCU designates a DTTU.

IFAL-DTT - Final Address Level From Terminal

When true, indicates that the Final Character of the Buffer is being addressed.

INnL-DTT - Input Information Level From Terminal

When true, an INnL (n = 1, 2, 4, 8, A, B) signal denotes a 1-bit in the corresponding position of a Character Code is being sent from the Terminal.

IRRL/-DTT - Inquiry Read-Ready Level From Terminal

When true, the Buffer Control Word of the designated Adapter indicates Read-Ready.

ISYL/-DTT - Initiate Sync Operation Level To Terminal

When false, signifies that the System is beginning the execution of a Data Communication Instruction.

ITCL/-DTT - Terminal Character Time Level

When false, indicates that the DTTU has received or is ready to transfer a character to the DTCU.

ITDL/-DTT - Terminal Designated Level

When false, an ITDL/-NN (01 thru 15) will be sent to the Terminal Unit designated by the DTCU "S" Register.

IWRL-DTT - Write-Ready Level From Terminal

When true, the Buffer Control Word of the designated Adapter indicates Write-Ready.

OInL/-DTT - Output Information Bits To Terminal

When false, an OInL (n = 1, 2, 4, 8, A, B) signal denotes a 1-bit in a corresponding position of a Character Code is sent to the Terminal.

RINL/-DTT - Read Inquiry Level To Terminal

When false, signifies that the Processing System is performing a Read Operation.

SIIL/-DTT - Set Interrupt Level From Terminal

When false, indicates that a Buffer requires attention of the Processing System.

TSnL/-DTT - Translation Selection Bits From Terminal

When false, the Translation Selection Levels (n = 1, 2) from the designated Terminal controls the type translation performed by the DTCU.

TUBL-DTT - Terminal Unit Busy Level From Terminal

When true, indicates the designated Terminal Buffer is Busy because:

1. The Buffer Control Word Busy bit (DA2F) is ON.
2. The Buffer Control Word indicates the Buffer is In Use by Adapter, DB6F ON.

TURL/-DTT - Terminal Unit Ready Level

When false, indicates the following:

1. The Terminal Unit is Ready - Power ON, Remote State.
2. An Adapter is connected to the addressed Buffer and the Not-Ready bit of the Buffer Control Word is OFF.

WIRL/-DTT - Write Inquiry Reply To Terminal

When false, signifies that the Processing System is performing a Write Operation.

Functional Detail

B5500 DATA COMMUNICATIONS INTERROGATE

The Interrogate operation makes available to the Processing System the status of a specific Buffer (possible 16) within a specific DTTU (possible 15).

There are two types of Interrogate operations defined as follows:

1. ACTIVE - An Interrogate operation is considered Active if the DTTU Number Field of the Descriptor D (36 → 39) is NON-ZERO; that is, a specific DTTU and Buffer within that DTTU is addressed by the System.

2. PASSIVE - An Interrogate operation is considered Passive if the DTTU Number Field of the Descriptor D (36 → 39) is ZERO. A Passive Interrogate is used to locate a Buffer within a DTTU which has expressed the need for System Attention by sending an Interrupt to Central Control. In this case, both DTTU Number and Buffer Number are supplied to the System by the DTTU and DTCU and will appear in the appropriate fields of the Result Descriptor.

All Interrogate Descriptors, whether Active or Passive, have D30F ON and D24F OFF.

Figure II-1, B5500 Sync Interrogate, is a Block Diagram of actions which occur in the I/O Control, Data Transmission Control and Data Transmission Terminal Unit during an Interrogate operation.

Figure II-2 illustrates the same actions in Timing Diagram form.

I/O INITIATES INTERROGATE OPERATION

SC = 03 · CC = 05 · D40F/

Refer to Figures II-7 and II-8.

When a DTCU is used in conjunction with one or more DTTUs, the D40F Pluggable Option is removed allowing I/O Control to send both DTTU and Buffer number since up to 15 DTTUs may be connected to one DTCU. Refer to I/O III D.A. Schematic Page 63.04.37.0 for Pluggable Option.

SC = 05 · HOLF/

Transfer the DTTU number D (39 → 36) plus D40F (which will be a zero) to OB(A → 1) and produce Sync Level (ISYL). The "OB" Register now contains the following information for the DTCU:

OB(8 → 1) = DTTU Number (1 → 15)
OBAF = Zero (DTCU is present)
OBBF = Zero

Functional Detail

I/O Control will remain in SC = 5 until ITCL (I24D) Inquiry Time for Character Level is generated by the DTCU.

DTCU RESPONSE TO ISYL

Refer to Figure II-9, SCAN - Begin Sync (P = 0).

P = 0 · Q = 0 · ISYL

With the DTCU in an Idle State (P = 0 · Q = 0) and the presence of SYNC (ISYL) from I/O Control, an A-Clock is produced which sets Q2F ON. Note that if the Scan Cycle is in progress, it is terminated by System Activity.

P = 0 · Q = 2 + 3 · ISYL

Another A-Clock is produced which loads the "A" Register (AQF ← 1) with the DTTU number from I/O Control and fires ATDM. Note that the "A" and "B" bit positions of the "A" Register are inhibited since the DTTU number is contained in the 1,2,4 and 8-bit positions only. The "S" Register is also loaded with the DTTU number provided the number is NON-ZERO. RESET SCAF, SET P = 4 and Q = 2.

P = 4 · Q = 2 · AQF · ISYL

Refer to Figure II-10, Sync Cycle (P = 4 + 5 + 6).

With the DTTU number in the "A" Register (AQF), System Sync (ISYL) and ATDM/; a B-Clock is produced.

The DTTU number is transferred from the "S" to the "B" Register, BQF is turned ON to mark the "B" Register occupied, and BTDM is fired.

The B-Time Delay Multi (BTDM) signals I/O Control that the DTTU number has been received by the DTCU and is now being returned.

BTDM produces Inquiry Time for Character Level (ITCL) which results in I24D in I/O Control.

I/O RESPONSE TO ITCL (I24D)

Inquiry Time for Character Level-Not (ITCS/) is sent to Central Control as a false level of 4μs. duration. ITCS/ is switched in Central Control and arrives in I/O as I24D and SETS SC = 4.

SC = 4 · I24S · EXNF/

Refer to Figure II-7, Data Communications I/O Flows

I/O Control remains in SC = 4 until ITCL goes false. During this period of time, IB(P → 1) is loaded with the DTTU number from the DTCU.

Functional Detail

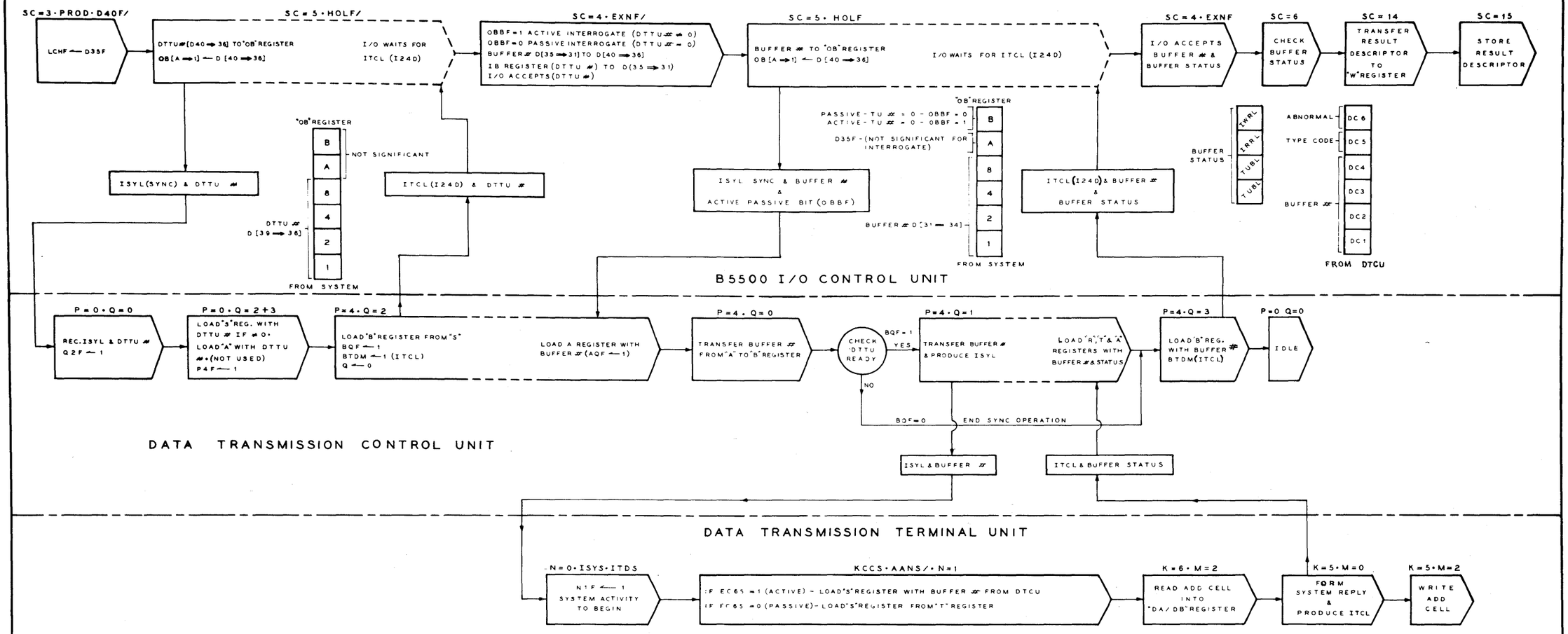


FIGURE II-1
B5500 DATA COMMUNICATIONS INTERROGATE

Functional Detail

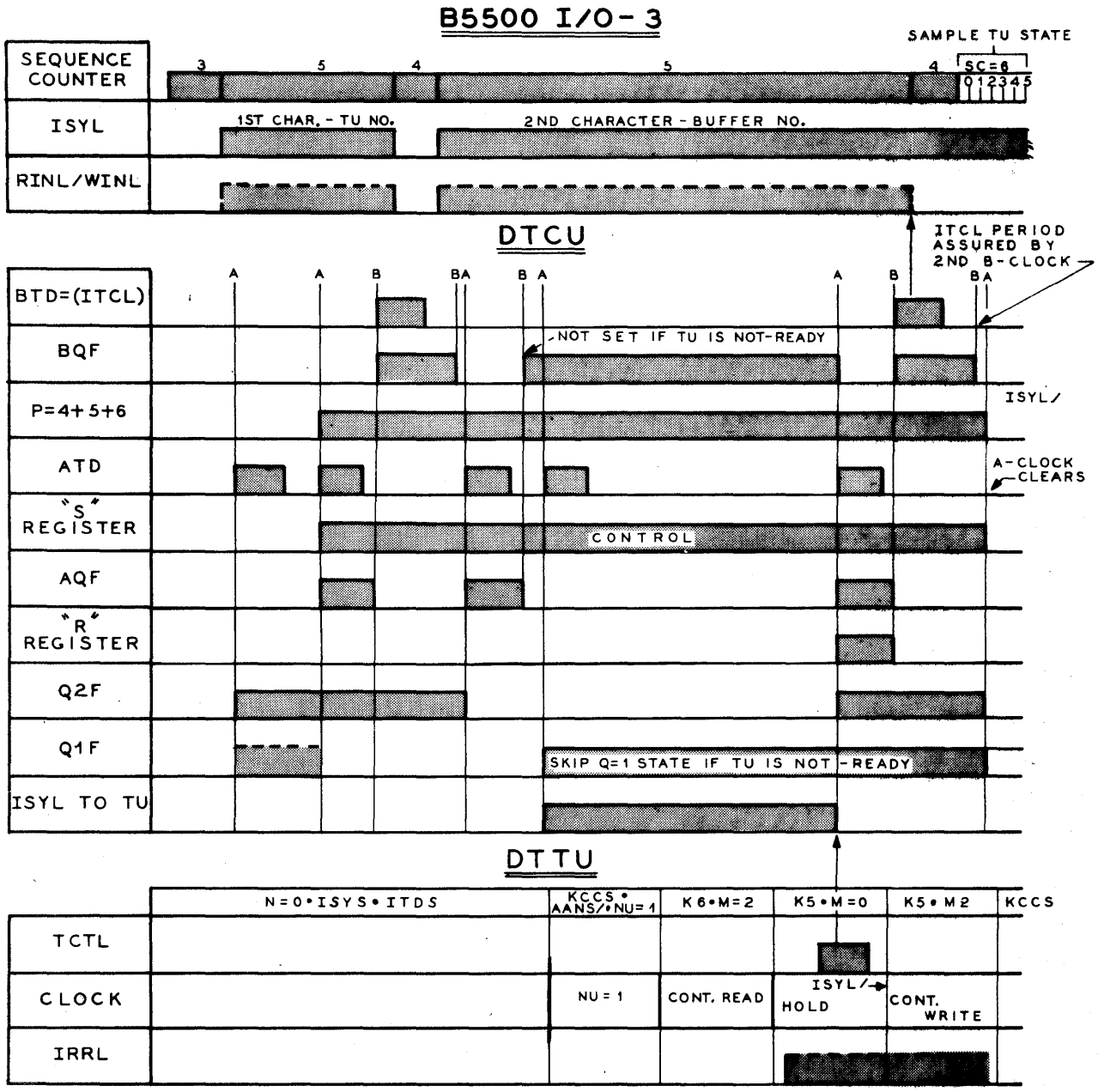


FIGURE II-2
B5500 DATA COMMUNICATION INTERROGATE TIMING

IB(A → 1) which contains the DTTU number is transferred to D (35 → 31). The Buffer number D(34 → 31) plus the Group Mark Significance bit D35F, is transferred to D(40 → 36). Note that D35F is significant only during System Read/Write and will be covered in that portion of System Activity.

If the DTTU number is NON-ZERO, set OBBF to specify Active Interrogate.

If the DTTU number is ZERO, OBBF is left reset to specify Passive Interrogate.

With I24S/ and EXNF/; turn HOLF ON, SET SC = 5, and send the Buffer number to the DTCU.

SC = 5 · HOLF

Transfer the Buffer number D(39 → 36) plus the Group Mark Significance bit (D35F) to OB(A → 1).

The "OB" Register now contains the following information:

OB(8 → 1) = Buffer Number
OBAF = Group Mark Significance bit (Not used for Interrogate)
OBBF = 1 Active Interrogate
OBBF = 0 Passive Interrogate

I/O Control again supplies ISYL and waits in SC = 5 for I24D from the DTCU.

DTCU RECEIVES BUFFER NUMBER

P = 4 · Q = 2 · AQF/

Refer to Figure II-10, Sync Cycle (P = 4 + 5 + 6).

An A-Clock is produced which loads the "A" Register with the Buffer number, turns AQF ON, and fires ATDM.

P = 4 · Q = 0 · ATDM/

With the A-Time Delay period past, a B-Clock is produced which transfers the Buffer number from "A" to "B" Register, RESETS AQF and, if the Terminal Unit is Ready (TURL), SETS BQF ON.

P = 4 · Q = 0 · AQF/

If BQF is ON, indicating that the DTTU is Ready, an A-Clock is produced which SETS Q = 1 and transfers the Buffer number to the Terminal Unit and the Interrogate operation proceeds.

If BQF is OFF, indicating that the DTTU is Not-Ready or Not Present, SET Q = 3, turn AQF ON, and SET R1F ON to reflect a DTTU Not-Ready or Not-Present condition, and terminate the Interrogate operation.

P = 4 · Q = 1

Refer to Figure II-10, Sync Cycle (P = 4 + 5 + 6).

The DTCU supplies ISYL and waits for the DTTU to respond with the TCTL (DTTU Character Time Level).

Functional Detail

DTTU RESPONSE TO ISYL

N = 0 · (ISYS) · ITDS

When the ISYL/ level goes false, ISYS in the DTTU will go true and SET the "N" Register to 1 provided N = 0.

KCCS · AANS/ · NU = 1

Refer to Figure II-13.

If no Adapter requires attention, the DTTU samples the Information sent by the DTCU to determine if an Active or Passive Interrogate is being called for. This Information is now contained in ECS[6 => 1] located in the DTTU. EC6S in particular, is sampled since it reflects the numeric value of the Buffer Number Field of the initiating Descriptor.

If EC6S is true, the Buffer number does NOT equal 0 and an Active Interrogate is begun by transferring ECnS[8 => 1] (Buffer number) to the "S" Register.

If EC6S/ is true, the Buffer number equals 0 and a Passive Interrogate is begun by transferring the "T" Register to the "S" Register. "T" contains the number of the Buffer which requires System Attention. This Buffer number will be returned to the System via the DTCU and will appear in the Buffer Number Field of the Result Descriptor.

K = 6 · M = 2 · N4F/

Refer to Figure II-14.

Read the contents of the Address Cell into the "D" Register. Had this been a Read or Write operation, RINS or WINS would be true at this time and the Group Mark Significance bit (AC5S) would be sampled. However, for an Interrogate operation, no other action occurs except for loading the "D" Register with the contents of the Address Cell and setting K = 5 · M = 0.

K = 5 · M = 0

Refer to Figure II- 15.

The Address Cell which is now in the "D" Register can either contain Addressing Information or Control Information. If DB6F is ON, the "D" Register contains Address Information. If DB6F is OFF, the "D" Register contains Control Information.

If the contents of the Address Cell contains Address Information, DA1F => DA4F are NOT sent to the DTCU. Instead, TUBL will be returned to the DTCU along with the present "S" Register setting (Buffer number) and DB1F (ABC).

If the contents of the Address Cell contains Control Information, DA1F

=> DA4F are sent to the DTCU (TURL/, TUBL, IRRL and IWRL) along with the contents of the "S" Register (Buffer number).

Since the status of the Buffer being interrogated is present only in the Control Word [DA1F => DA4F], the contents of these four bit positions are sent to the System only when DB6F is OFF.

If the Buffer is found to be Interrupt (DA6F), RESET N8F; and if this is a Passive Interrogate, RESET DA6F. SET N2F to initiate a Scan Cycle to determine if any other Buffer requires System Attention.

Generate TCTL and SET M = 2.

K = 5 · M = 2

Write the contents of the "D" Register into the Address Cell location and go to KCCS (Idle).

DTCU RESPONSE TO TCTL

P = 4 · Q = 1 · TCTL

Refer to Figure II-10, Page 2 of 2.

The Terminal Character Time Level (TCTL) from the DTCU generates an A-Clock which loads the "A" Register with the Buffer number from the DTTU and loads the "R" and "T" Registers with the Buffer status and type of Translation required for this particular Buffer.

Fire ATDM and SET Q = 3.

P = 4 · Q = 3

After ATDM has timed out, a B-Clock is generated which loads the "B" Register with the Buffer number (BQF ← 1) and fires BTDM.

BTDM signals I/O Control to accept the information from DTCU.

A second B-Clock is produced which RESETS BQF to indicate that I/O has taken the Information.

With BQF OFF, an A-Clock is generated which clears the DTCU and terminates the Sync Interrogate operation as far as the DTCU is concerned.

I/O RESPONSE TO ITCL

Inquiry Time for Character Level-Not (ITCS/) is sent to Central Control as a false level of 4μs. duration. ITCS/ is switched in Central Control and arrives in I/O as I24D which SETS SC = 4. Refer to Figure II-7.

SC = 4 · I24S · EXNF

I/O Control remains in SC = 4 for 4μs, or, until ITCL goes false. During this period of time, IB[P => 1] is loaded with Information from the DTCU.

IB[A => 1] which contains Buffer number plus type of Adapter Information, is transferred to the Buffer Number Field of the Result Descriptor D[35 => 31].

The DTTU Number Field which has been temporarily stored in D[35 => 31] is transferred to its original bit position D[40 => 36]. When ITCL goes false, I24S will again go true and, with EXNF ON, SETS SC = 6.

SC = 6

IBBF now contains the status of the Adapter Abnormal bit (ABC) and if the Buffer was Abnormal during the Interrogate operation, EXNF is RESET to remember this condition.

If an Abnormal Condition (ABC) was present during the Interrogate Operation, the DTCU reply to the System would cause IBBF to be ON at this time. IBBF ON at SC = 6 will cause EXNF to be RESET and D25F will be SET in the Result Descriptor to reflect this condition.

The Character Counter is allowed to count from CC = 0 to CC = 4 during which time the Result Descriptor will be formed to reflect the condition of the Buffer that was interrogated.

CC = 1 - RESET D18F and SET D20F if the DTTU Buffer was Not-Ready.

CC = 3 - SET D20F if the DTTU Buffer was Busy.

SET D21F if an Interrogate found the DTTU Buffer Write-Ready.

SET D24F if an Interrogate found the DTTU Buffer Read-Ready.

Exit to SC = 14 and store the Result Descriptor.

The Interrogate operation is complete at this point since the latest Buffer conditions are now contained in the Result Descriptor.

B5500 DATA COMMUNICATIONS READ

All Read Descriptors have D30F OFF and D24F ON. Refer to Figure II-3, B5500 Data Communications Read which is a Block Diagram of events which occur in the I/O Control, Data Transmission Control and Data Transmission Terminal Unit during a Read operation.

Figure II-4, Read Transfer Timing Diagram, illustrates Information Transfer after Sync has been accomplished.

Normal entry to the Data Communications Flow is made through the Standard Sequence Count Logics. Assume D16F and D18F are both ON, and the

Character Counter has been incremented to 5. Refer to Figures II-7 & II-8, Data Communications I/O Flows.

I/O INITIATES READ OPERATION

SC = 3 · CC = 5 · D40F/

When a DTCU is used in conjunction with one or more DTTUs, the D40F Pluggable Option is removed allowing I/O Control to send both DTTU and Buffer Number since up to 15 DTTUs may be connected to one DTCU. Refer to I/O III D.A. Schematic Page 63.04.37.0 for Pluggable Option.

SC = 5 · HOLF/

Transfer the DTTU number D[39 => 36] plus D40F (which will be a zero) to OB[A => 1] and produce Sync Level (ISYL) and Read Level (RINL). The "OB" Register now contains the following Information for the DTCU.

OB[8 => 1] = DTTU Number [1 => 15].
OBAF = Zero (DTCU present).
OBBF = Zero.

I/O will remain in SC = 5 until ITCL (I24D) Inquiry Time for Character Level is generated by the DTCU.

DTCU RESPONSE TO ISYL & RINL

Refer to Figure II-9, SCAN: Begin Sync (P = 0).

P = 0 · Q = 0 · ISYL · RINL

With the DTCU in an Idle State (P = 0 · Q = 0) and the presence of SYNC (ISYL) from I/O Control, and A-Clock is produced which SETS Q2F ON. Note that if a Scan Cycle is in progress, it is terminated by System Activity.

P = 0 · Q = 2 + 3 · ISYL · RINL

Another A-Clock is produced which loads the "A" Register (AQF ← 1) with the DTTU number from I/O Control and fires ATDM (A-Time Delay Multi). Note that the "A" and "B" bit positions of the "A" Register are ignored since the DTTU number is contained in the 1,2, 4 and 8-bit positions only. The "S" Register is also loaded with the DTTU number provided the number is NON-ZERO.

RESET SCAF, SET P = 5 and Q = 2.

P = 5 · Q = 2 · AQF · ISYL · RINL

Refer to Figure II-10, Page 1 of 2.

With the DTTU number in the "A" Register (AQF), System Sync (ISYL) and

Functional Detail

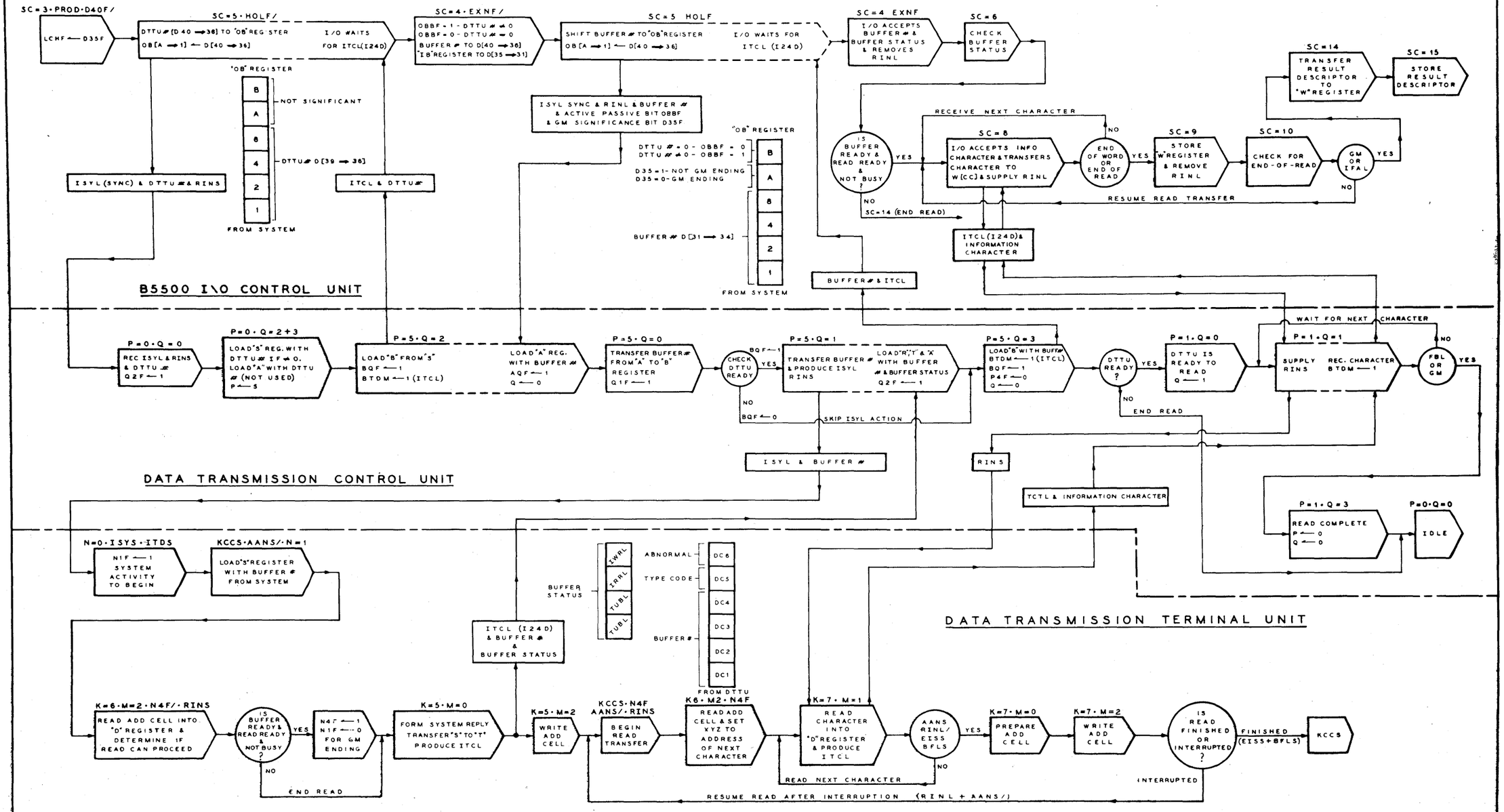


FIGURE II-3
B5500 DATA COMMUNICATIONS READ

Functional Detail

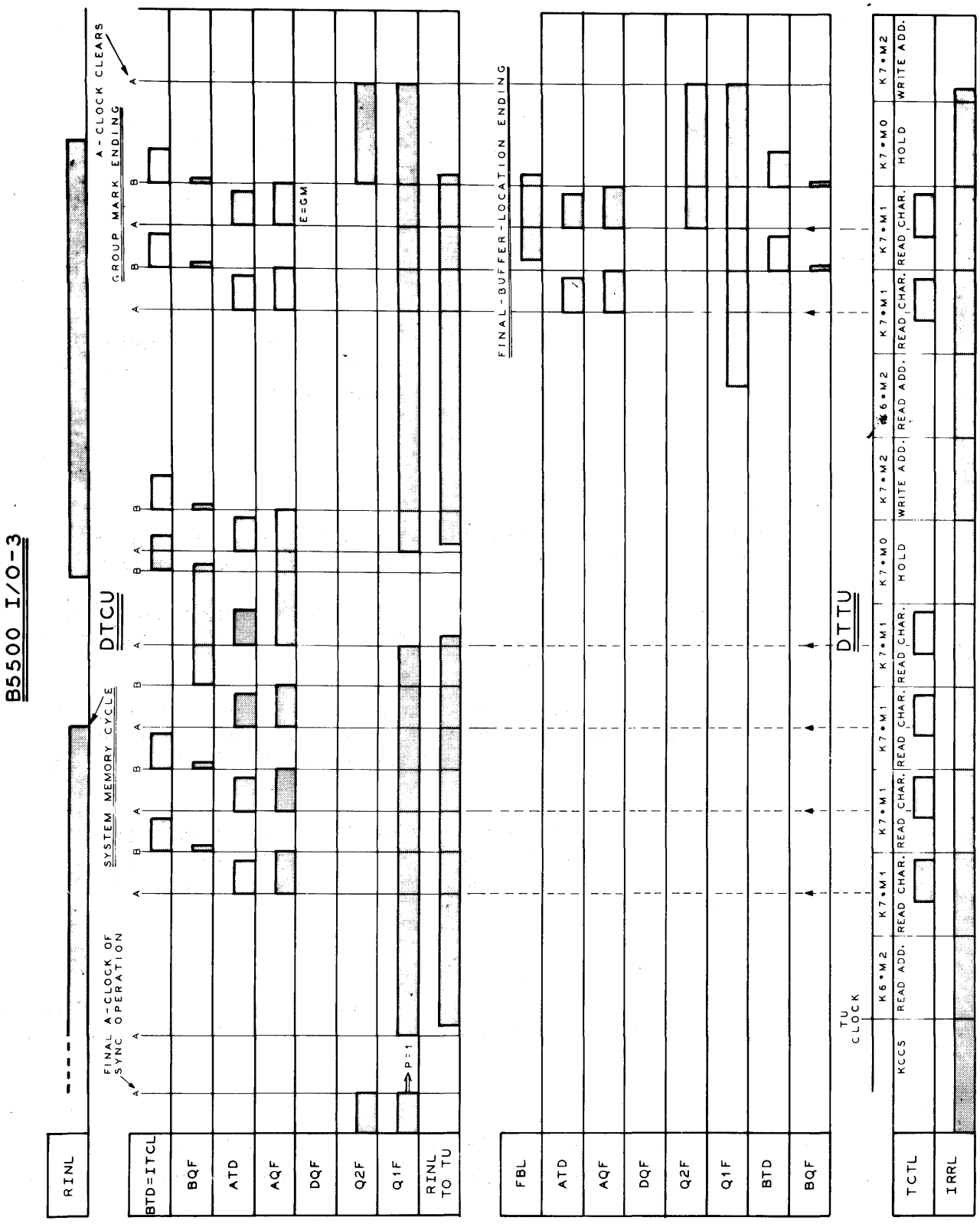


FIGURE II-4
B5500 DATA COMMUNICATIONS READ TIMING

ATDM/, a B-Clock is produced.

The DTTU number is transferred form the "S" Register to the "B" Register, BQF is turned ON to mark the "B" Register "occupied" and BTDM is fired.

The B-Time Delay Multi (BTDM) signals I/O Control that the DTTU number has been received by the DTCU and is now being returned.

BTDM produces Inquiry Time for Character Level (ITCL) which results in I24D in I/O Control.

I/O RESPONSE TO ITCL (I24D)

Inquiry Time for Character Level-Not (ITCS/) is sent to Central Control as a false level of 4μs. duration. ITCS/ is switched in Central Control and arrives in I/O Control as I24D and SETS SC = 4.

SC = 4 · I24S · EXNF/

Refer to Figure II-7.

I/O Control remains in SC = 4 until ITCL goes false. During this 4μs. period, IB[P => 1] is loaded with the DTTU number from the DTCU.

IB[A => 1] which contains the DTTU number is transferred to D[35 => 31]. The Buffer number D[34 => 31], plus the Group Mark Significance bit D35F, is transferred to D[40 => 36].

Note that for a Read operation, D35F is used to specify whether the Read Transfer is to terminate when a Group Mark is encountered or to ignore a Group Mark character and terminate when the Buffer Final Address is reached.

If the numeric value of the DTTU Number Field is NOT equal to zero, OBBF is SET to 1. This will serve as a Flag in the DTTU that the System is supplying a specific Buffer number. All Read Descriptors should have a NON-ZERO number in this field.

SC = 5 · HOLF · D30F/

Transfer the Buffer number D[39 => 36] plus the Group Mark Significance bit to OB[A => 1]. The "OB" Register now contains the following Information:

OB[8 => 1] = Buffer number.

OBAF = Group Mark Significance bit (based on D35F).

OBAF = 1 = Ignore Group Mark character and read to Buffer Final Address.

OBAF = 0 = Terminate the Read operation when a Group Mark is encountered.

OBBF = 1 = System is supplying a Buffer number.

Functional Detail

The Information contained in the "OB" Register is transferred to the DTCU. Sync Level (ISYL) and RINL are also produced at this time and sent to the DTCU. The I/O Channel remains in SC = 5 until ITCL (Inquiry Time for Character Level) is generated by the DTCU. This is to allow the DTTU time to form a reply for the System as to the status of the Buffer-To-Be-Read.

DTCU RECEIVES BUFFER NUMBER

P = 5 · Q = 2 · AQF/

Refer to Figure II-10, Sync Cycle (P = 4 + 5 + 6) Page 1 of 2.

An A-Clock is produced which loads the "A" Register with the Buffer number, turns AQF ON, fires ATDM, and SETS Q = 0.

P = 5 · Q = 0 · ATDM/

If BQF is ON indicating that the DTTU is Ready, an A-Clock is produced which SETS Q = 1, it transfers the Buffer number to the DTTU, and the Read operation proceeds.

If BQF is OFF (DTTU Not-Ready or Not Present); SET Q = 3, turn AQF ON, and SET R1F ON to reflect this condition.

P = 5 · Q = 1 · RINL

Refer to Figure II-10, Page 2 of 2.

The DTCU supplies ISYL and RINL to the DTTU and waits for the DTTU to respond with TCTL (DTTU Character Time Level).

DTTU RESPONSE TO ISYL & RINS

N = 0 · (ISYS) · ITDS · RINS

When the ISYL/ level goes false, ISYS in the DTTU will go true and SET the "N" Register to 1 provided N = 0.

KCCS · AANS/ · NU = 1

Refer to Figure II-13, KCCS - Idle/Scan Flow.

If no Adapter requires Attention (AANS/), the DTTU samples the Information sent by the DTCU. Since the System always supplies a Buffer number for a Read operation, EC6S will be true, causing the Buffer number to be transferred to the "S" Register. The "K" and "M" Registers are SET to 6 and 2 respectively to allow DTTU access to the ADD cell.

K = 6 · M = 2 · RINS · NU = 1

Refer to Figure II-14, Begin System Sync Cycle.

Read the contents of the ADD cell into the "DA" and "DB" Registers. The presence of the Read Level (RINL) from DTCU will cause N4F to be SET provided either of the following conditions exist:

1. DB6F/ · DM00G - The ADD cell does not contain Address Information (DB6F/), and the Buffer is Idle (DM00G).

2. DB6F/ · DA3F · WIRL/ - The ADD cell does not contain Address Information (DB6F/), the Buffer is Read-Ready (DA3F), and the System is not attempting a Write operation (WIRL/).

If the above conditions are not met, N4F will not be SET and the Result Descriptors will reflect the fact that the Read operation can not be performed.

The Group Mark Significance bit now contained in EC5S, is also sampled at this time. If EC5S/ is true, N1F is RESET which will cause the Read operation to be terminated when a Group Mark character is encountered. If EC5S is true, N1F is NOT RESET and the Read operation is NOT terminated when a Group Mark character is encountered but continues until Buffer Final Address is reached.

The DTTU now proceeds to K = 5 · M = 0 in order to form a reply to the System as to the status of the Buffer to be read and to produce TCTL for the DTCU.

K = 5 · M = 0 · N4F

Refer to Figure II-15, Sync Cycle.

The contents of the ADD cell now in the "D" Register, can either contain Address Information or Control Information. If DB6F is ON, the "D" Register contains Address Information. If DB6F is OFF, the "D" Register contains Control Information.

Since the status of the Buffer-To-Be-Read is present only in the Control Word DA[1 => 4], the contents of these four bit positions are sent to the System only when DB6F is OFF.

If the contents of the ADD cell contains Address Information, DA[1 => 4] are not sent to the System. Instead, TUBL (Terminal Unit Busy Level) will be returned to the System along with the present "S" Register contents (Buffer number) and DB1F (ABC).

If the Address Cell contains Control Information, DA[1 => 4] is sent to the System (TURL/, TUBL, IRRL and IWRL) along with the present "S" Register contents (Buffer number) and DB1F (ABC).

If the Read operation is to proceed (N4F ON), the "D" Register is cleared with the exception of DA6F and DB6F which are turned ON to

mark this Buffer In-Use-By-System.

The "S" Register is transferred to the "T" Register since it is possible that the "S" Register could be changed by some Adapter-Attention-Needed (AANS) before the actual Read Transfer begins. The DTCU now proceeds to K = 5 · M = 2 to store the "D" Register into the ADD cell location.

TCTL (Terminal Character Time Level) is sent to the DTCU along with the Buffer status bits and the Buffer number.

K = 5 · M = 2

Write the ADD cell and proceed to KCCS with N4F ON.

DTCU RESPONSE TO TCTL

P = 5 · Q = 1 · TCTL

Refer to Figure II-10, Sync Cycle (P = 4 + 5 + 6) Page 2 of 2.

The Terminal Character Time Level (TCTL) from the DTTU, generates an A-Clock which loads the "A" Register with the Buffer number from the DTTU and loads the "R" and "T" Registers with the Buffer status and type of Translation required for this particular Buffer.

Fire ATDM and SET Q = 3.

P = 5 · Q = 3

After ATDM has timed out, a B-Clock is generated which transfers the Buffer number from "A" to "B" (BQF ← 1) and fires BTDM. BTDM signals I/O Control to accept the Information from the DTCU.

A second B-Clock is produced which RESETS BQF to indicate that I/O has taken the Information. RESET the "Q" Register and P4F. The DTCU is now ready for the Read Transfer to begin.

I/O RESPONSE TO ITCL

Inquiry Time for Character Level-Not (ITCS/) is sent to Central Control as a false level of 4μs. duration. ITCS/ is switched in Central Control and arrives in I/O as I24D which SETS SC = 4. Refer to Figure II-7.

SC = 4 . I24S · EXNF

I/O Control remains in SC = 4 for 4μs. or, until ITCL goes false. During this period of time, IB[P => 1] is loaded with Information from the DTCU.

IB[A => 1] which contains Buffer number plus type of Adapter Information, is transferred to the Buffer Number Field of the Result Descrip-

tor D[35 => 31].

The DTTU number which has been temporarily stored in D[35 => 31] is transferred to its original bit position D[40 => 36]. When ITCL goes false, I24S will again go true and, with EXNF ON, SETS SC = 6.

SC = 6 · D24D

IBBF now contains the status of the Abnormal bit (ABC) and if the Buffer was Abnormal (DB1F = 1), EXNF is RESET to remember this condition.

The Character Counter is allowed to count from CC = 0 to CC = 5 during which time the Result Descriptor is formed to reflect the status of the Buffer to be read.

CC = 1 - RESET D18F and SET D20F if the Buffer was found Not-Ready

CC = 3 - SET D20F if the Buffer was Busy. SET D21F if the Buffer was found Write-Ready when a Read was attempted.

CC = 4 - Terminate the Read operation if the Buffer was found Busy, Not-Ready, or Not Read-Ready.

If EXNF had been RESET due to an Abnormal Condition, D25F is SET in the Result Descriptor.

The Character Counter will be counted to CC = 5 only if the Read operation can proceed. With CC = 5 and D24D (Read), the Sequence Counter is SET to SC = 8.

I/O Control waits at SC = 8 for ITCL plus an Information character to arrive from the DTCU.

READ TRANSFER (DTTU)

KCCS · N4F · AANS/

Refer to Figure II-13, KCCS - Idle Scan Flow.

N4F ON, No-Adapter-Attention-Needed, and KCCS will SET K = 6 · M = 2. This initiates a Read Access on the ADD cell location. The first time the ADD cell is found cleared (DM00G, the "S" Register is transferred to the "Y" Register to select the Buffer Plane, while X2F is SET to address the first character position in that Buffer. Refer to Figure II-16.

K = 7 · M = 1

Refer to Figure II-17, Read Transfer to System.

The first two characters are read into the "DA" and "DB" Registers. Z1F OFF causes the character in "DA" to be sent to the DTCU first.

Inquiry Time for Character Switch-Not (ITCS/) goes false 4μs. after the Clock pulse that initiated the Memory cycle and remains false for

a period of 4μs.

ITCS/ going false in the DTTU causes TCTL to go true in the DTCU. In this manner, the DTTU signals the DTCU that a character has been read from Buffer Memory.

The process of reading a character at a time from Buffer Memory and presenting the character to the DTCU along with TCTL, continues until one of the following conditions occur:

1. GM - A Group Mark Character is read from Buffer Memory and a Group Mark Ending was specified in the Read Descriptor.
2. BFAL - Buffer Final Address has been reached.
3. AAN = 1 - Some Adapter Requires Attention.

or RIN = 0 - System Memory Cycle.

In the event of AAN = 1 or RIN = 0, the DTTU updates the Add Cell with the present "X", "Y", "Z" settings to indicate where Read Transfer was interrupted. Read Transfer resumes from this point after the Adapter requiring Attention has been serviced or the B5500 Memory Cycle is complete.

DTCU RECEIVES TCTL & INFORMATION CHARACTER

P = 1 · Q = 1 · TCTL

Refer to Figure II-11, Read (P = 1).

An A-Clock is generated which loads the "A" Register with the Information Character from the DTTU, fires ATDM, and turns AQF ON.

P = 1 · BQF = 0 · AQF = 1 · ATDM/

When ATDM has timed out, a B-Clock is generated which transfers the Information character from "A" to "B", turns AQF OFF, BQF ON, and fires BTDM. Note that the ATDM period insures sufficient delay for translation as specified by the "T" Register.

BTDM signals I/O Control that an Information character is being presented by the DTCU by generating I24D.

The process of receiving a character at a time from the DTTU, translating the character if specified, and presenting the character to I/O Control, continues until one of the following conditions occur:

1. - A Group Mark Character is received from the DTTU and a Group Mark Ending was specified in the Read Descriptor. In this case, "Q" is SET to 3 with the same B-Clock that transfers the Group Mark character from "A" to "B". With P = 1 · Q = 3, an A-Clock is generated which clears the DTCU, thus terminating the Read operation.

Functional Detail

2. FBL - Final Buffer Location has been reached. When the last character position is addressed, the DTTU generates FBL which in turn SETS Q = 3 in the DTCU at A-Clock time. With P = 1 · Q = 3 · EGM = 0 (not GM), an A-Clock is produced that clears the DTCU and generates IFAL (I23D) in I/O Control.

3. RINL/ - B5500 Memory Cycle. When eight characters have been accumulated in the "W" Register of I/O Control, a Memory Cycle is initiated to store this word in System Memory. When I/O Control leaves SC = 8 to perform the Memory Write, RINL goes false. However, the DTCU continues to load the "A" and "B" Registers and merely waits for RINL to reappear. This is accomplished by inhibiting BTDM until I/O Control has performed the Memory Write and has returned to SC = 8 and again supplies RINL.

I/O CONTROL RECEIVES INFORMATION CHARACTERS

SC = 8 · RINL

Refer to Figure II-8.

The first B5500 Clock pulse with I24D (ITCL) turns STRF ON. The next Clock pulse with STRF ON, SETS IB[B => 1] with the character on the IN[B => 1] lines and turns HOLF ON.

With HOLF ON and D17F OFF (Not End-Of-Word or End-Of-Read), RINL will go false. Thus, RINL goes false once per character time or until HOLF is RESET by I24S/ going true.

The next Clock pulse with HOLF and STRF ON, transfers the character in "IB" to the character position in the "W" Register as specified by the Character Counter. STRF and "IB" are cleared.

The Character Counter is incremented by one to store the contents of the "W" Register into System Memory.

I23D becomes true in I/O Control if the Final Address of the DTTU Buffer is reached (IFAL true). I23D causes LPPF to be SET. The next Clock pulse with LPPF ON causes D17F to be SET. D17F is used as a Logical Flip-flop to produce SC + 1 so that the contents of the "W" Register can be stored at SC = 9.

LCHF ON enables logic to Ignore-Group-Mark. LCHF causes AGMS (Allow-Group-Mark-Switch) to be held false and prevent GPMS from ever becomming true. The Group Mark is handled like any other character and written into Memory.

If LCHF is OFF, a Group Mark Character in the "IB" Register causes GPMS to become true and SET D17F. D17F again produces SC + 1 and stores the "W" Register at SC = 9.

SC = 9

The Character Counter is cleared and the Memory-Access-Needed Flip-flop is SET. The Memory Write Driver (MWRD) and Memory Timing Zero Driver (MTOD) SETS the Memory-Access-Obtained Flip-flop to indicate that the word in the "W" Register is now stored. MAOF and the "W" Register are cleared with the next Clock pulse and the Sequence Counter is SET to 10.

SC = 10

If End-Of-Buffer has not been detected (LPPF/), and if no Group Mark is encountered, the Sequence Counter is SET to 8 to load the "W" Register with the next word.

If a Group Mark Character was detected (and Group Mark Ending specified) or a Buffer Final Address detected, SET SC = 14 and terminate the Read operation.

B5500 DATA COMMUNICATIONS WRITE

All Data Communications Write Descriptors have D30F OFF and D24F OFF.

Figure II-5, Data Communications Write, is a Block Diagram of events which occur in I/O Control, Data Transmission Control and the Data Transmission Terminal Unit during a Write operation.

Figure II-6, Write Transfer Timing Diagram, illustrates Information Transfer after Sync has been established with the DTTU. The Group Mark and Buffer Full End plus a Write Transfer interruption by a System Memory Cycle is also shown.

Normal entry to the Data Communications Flow is made through the Standard Sequence Count Logics. Assume that D16F and D18F are both ON and the Character Counter has been counted to 5. Refer to Figures II-7 and II-8 which are Data Communications I/O Flows.

I/O INITIATES WRITE OPERATION

SC = 3 · CC = 5 · D40F/

When a DTCU is used in conjunction with one or more DTTUs, the D40F Pluggable Option is removed allowing I/O Control to send both DTTU and Buffer number since up to 15 DTTUs may be connected to one DTCU. Refer to I/O D.A. Schematic, Page 63.04.37.0 for Pluggable Option.

SC = 5 · HOLF/

Transfer the DTTU number D[39 => 36] plus D40F (which will be zero) to OB[A => 1] and produce Sync (ISYL) and Write (WIRL) Levels. The "OB" Register now contains the following Information for the DTCU:

Functional Detail

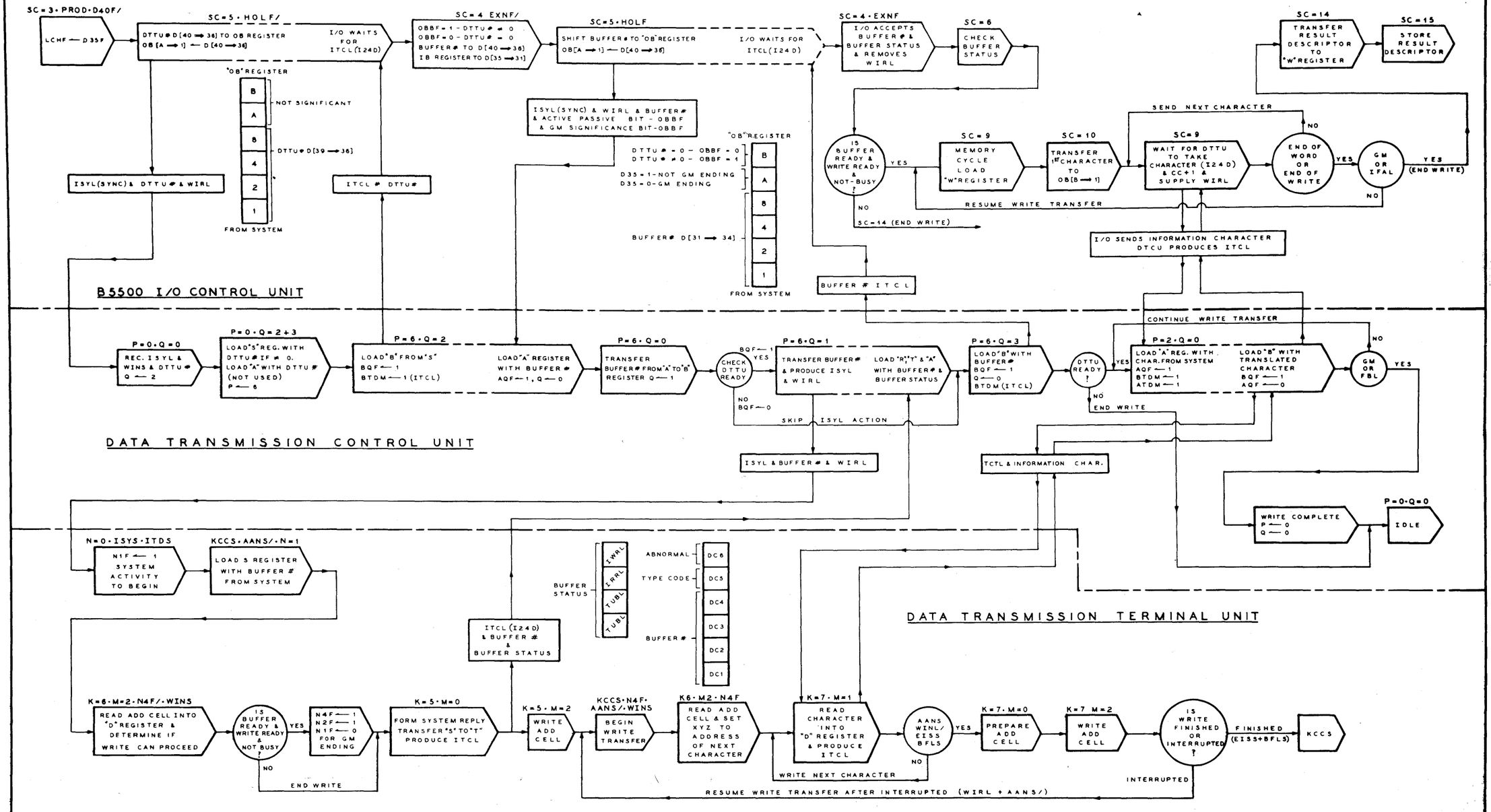


FIGURE II-5

B5500 DATA COMMUNICATIONS WRITE

OB[8 => 1] = DTTU number [1 => 15].

OBAF = Zero (DTTU present).

OBBF = Zero.

I/O Control will remain in SC = 5 until ITCL (I24D), Inquiry Time For Character Level is generated by the DTCU.

DTCU RESPONSE TO ISYL & WIRL

Refer to Figure II-9, SCAN - Begin Sync (P = 0).

P = 0 · Q = 0 · ISYL · WIRL

With the DTCU in an Idle State (P = 0 · Q = 0) and the presence of Sync (ISYL) from I/O Control, an A-Clock is produced which SETS Q2F ON. Note that if a Scan Cycle is in progress, it is terminated by System Activity.

P = 0 · Q = 2 + 3 · WIRL

Another A-Clock is produced which loads the "A" Register (AQF ← 1) with the DTTU number from I/O Control and fires ATDM (A-Time Delay Multi). Note that the "A" and "B" bit positions of the "A" Register are ignored since the DTTU number is contained in the 1,2,4 and 8-bit positions only.

The "S" Register is also loaded with the DTTU number provided the number is a NON-ZERO. RESET SCAF, SET P = 0 · Q = 2.

P = 6 · Q = 2 · ISYL · WINL

Refer to Figure II-10, Page 1 of 2.

With the DTTU number in the "A" Register (AQF), System Sync (ISYL) and ATDM/; a B-Clock is produced.

The DTTU number is transferred from the "S" to the "B" Register, BQF is turned ON to mark the "B" Register Occupied, and BTDM is fired.

The B-Time Delay Multi (BTDM) signals I/O Control that the DTTU number has been received by the DTCU and is now being returned.

BTDM produces Inquiry Time For Character Level (ITCL) which results in I24D in I/O Control.

I/O RESPONSE TO ITCL (I24D)

Inquiry Time for Character Level-Not (ITCS/) is sent to Central Control as a false level of 4μs. duration. ITCS/ is switched in Central Control and arrives in I/O Control as I24D and SETS SC = 4. Refer to Figure II-7.

Functional Detail

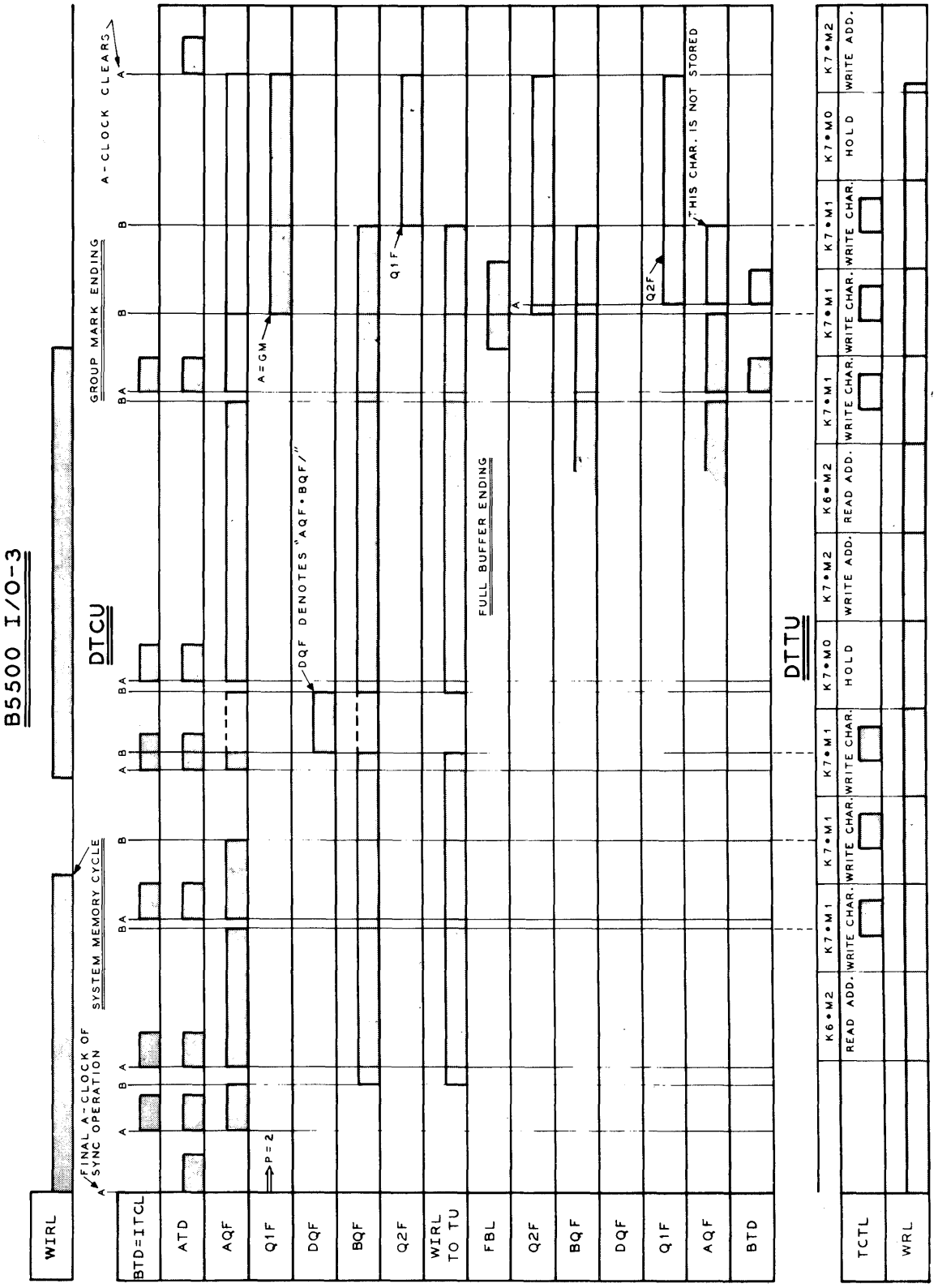


FIGURE II-6
B5500 DATA COMMUNICATIONS WRITE

SC = 4 · I24 · EXNF/

I/O Control remains in SC = 4 until ITCL goes false. During this 4μs. period, IB[P => 1] is loaded with the DTTU number from the DTCU.

IB[A => 1] which contains the DTTU number, is transferred to D[35 => 31]. The Buffer number D[34 => 31] plus the Group Mark Significance bit D35F, is transferred to D[40 => 36].

For a Write operation, D35F is used to specify whether the Write Transfer is to terminate when a Group Mark is encountered or to Ignore a Group Mark Character and terminate when Buffer-Final-Address is reached.

If the Numeric value of the DTTU number is NOT equal to 0, OBBF is SET to 1. This will serve as a Flag in the DTTU that the System is supplying a specific Buffer number. All Write Descriptors should have a NON-ZERO number in this field.

SC = 5 · HOLF · D30F/

Transfer the Buffer number D[39 => 36] plus the Group Mark Significance bit to OB[A => 1]. The "OB" Register now contains the following Information:

OB[8 => 1] = Buffer number.

OBAF = Group Mark Significance bit (based on D35F).

OBAF = 1 = Ignore Group Mark Character and Write to Buffer Final Address.

OBAF = 0 = Terminate the Write operation when a Group Mark Character is encountered.

OBBF = 1 = System is supplying a Buffer number.

The Information contained in the "OB" Register is transferred to the DTCU. Sync (ISYL) and Write (WINL) are also produced at this time and sent to the DTCU. I/O Control remains in SC = 5 until ITCL (Inquiry Time For Character Level) is generated by the DTCU. This is to allow the DTTU time to form a reply for the System as to the status of the Buffer to be written.

DTCU RECEIVES BUFFER NUMBER

P = 6 · Q = 2 · AQF/

Refer to Figure II-10. Sync Cycle (P = 4 + 5 + 6). Page 1 of 2.

An A-Clock is produced which loads the "A" Register with the Buffer number, turns AQF ON, fires ATDM, and SETS Q = 0.

P = 6 · Q = 0 · ATDM/

With the A-Time Delay period past, a B-Clock is produced which trans-

fers the Buffer number from "A" to "B", RESETS AQF and, if the Terminal Unit is Ready (TURL), SETS BQF ON.

P = 6 · Q = 0 · AQF/

If BQF is ON indicating that the DTTU is Ready; an A-Clock is produced which SETS Q = 1, transfers the Buffer number to the DTTU, and the Write operation proceeds.

If BQF is OFF (DTTU Not-Ready or Not Present), SET Q = 3, turn AQF ON, and SET R1F to reflect this condition in the Result Descriptor.

P = 6 · Q = 1 · WINL

Refer to Figure II-10, Page 2 of 2.

The DTCU supplies ISYL and WINL to the DTTU and waits for the DTTU to respond with TCTL (Terminal Unit Character Time Level).

DTTU RESPONSE TO ISYL & WINS

N = 0 · (ISYS) · ITDS · WINS

When the ISYL/ level goes false, ISYS in the DTTU will go true and SET the "N" Register to 1 provided N = 0.

KCCS · AANS/ · NU = 1

Refer to Figure II-13, KCCS - Idle/Scan Flow.

If no Adapter requires attention (AANS/), the DTTU samples the Information sent by the DTCU. Since the System always supplies a Buffer number for a Write operation, EC6S will be true causing the Buffer number to be transferred to the "S" Register.

The "K" and "M" Registers are SET to 6 and 2 respectively to allow DTTU access to the Add Cell.

K = 6 · M = 2 · WINS · NU = 1

Refer to Figure II-14, Begin System Sync Cycle.

Read the contents of the Add Cell into the "DA" and "DB" Register. The presence of the Write level (WINL) from DTCU will cause N4F and N2F to be SET provided either of the following conditions exist:

1. DB6F/ · DM00G - The Add Cell does not contain Address Information (DB6F/) and the Buffer is Idle (DM00G).

2. DB6F/ · DA4F · RINL/ - The Add Cell does not contain Address Information (DB6F/), the Buffer is Write-Ready (DA4F) and the System is not attempting a Read operation (RINL/).

If the above conditions are not met, N4F and N2F will not be SET and the Result Descriptor will reflect the fact that the Write operation cannot be performed.

The Group Mark Significance bit now contained in EC5S, is also sampled at this time. If EC5S/ is true, N1F is RESET which will cause the Write operation to be terminated when a Group Mark Character is encountered.

If EC5S is true, N1F is NOT RESET and the Write Operation is not terminated when a Group Mark Character is encountered, but continues until Buffer Final Address is reached.

The DTTU now proceeds to K = 5 · M = 0 in order to form a reply to the System as to the status of the Buffer to be Written and to produce TCTL for the DTCU.

K = 5 · M = 0 · N4F

Refer to Figure II-15, Sync Cycle.

The contents of the Add Cell which are now in the "D" Register, can either contain Address Information or Control Information. If DB6F is ON, the "D" Register contains Address Information. If DB6F is OFF, the "D" Register contains Control Information.

Since the status of the Buffer to be Written is present only in the Control Word DA[1 => 4], the contents of these four bit positions are sent to the System only when DB6F is OFF.

If the contents of the Add Cell contain Address Information, DA[1 => 4] are not sent to the System. Instead, TUBL (Terminal Unit Busy Level) will be returned to the System along with the present "S" Register contents (Buffer number) and DB1F (ABC).

If the Address Cell does contain Control Information, DA[1 => 4] is sent to the System as (TURL/, TUBL, IRRL and IWRL) along with the present "S" Register contents (Buffer number) and DB1F (ABC).

If the Write operation is to proceed (N4F ON), the "X", "Y" and "Z" is transferred to "D". DA6F and DB6F are turned ON to mark this Buffer In-Use-By-System.

The "S" Register is temporarily transferred to the "T" Register since it is possible that the "S" Register could be changed by some Adapter Attention Needed (AANS) before the actual Write Transfer begins. The DTTU now proceeds to K = 5 · M = 2 to store the "D" Register into the Add Cell location. TCTL (Terminal Character Time Level) is sent to the DTCU along with the Buffer status bits and the Buffer number.

K = 5 · M = 2

Write the contents of the "D" Register into the Add Cell location and proceed to KCCS with N4F ON. The DTTU is Ready for Write Transfer to begin.

Functional Detail

DTCU RESPONSE TO TCTL

P = 6 · Q = 1 · TCTL

Refer to Figure II-10, Page 2 of 2.

The Terminal Character Time Level (TCTL) from the DTTU generates an A-Clock which loads the "A" Register with Buffer number from the DTTU and loads the "R" and "T" Registers with the Buffer status and Type Of Translation required for this particular Buffer. Fire ATDM and SET Q = 3.

P = 6 · Q = 3

After ATDM has timed out, a B-Clock is generated which transfers the Buffer number from "A" to "B" and fires BTDM. BTDM signals I/O Control to accept the Information from DTCU.

A second B-Clock is produced which RESETS BQF to indicate that I/O has taken the Information.

RESET the "Q" Register and P4F. The DTCU is now Ready for the Write Transfer to begin.

I/O RESPONSE TO ITCL

Inquiry Time for Character Level-Not (ITCS/) is sent to Central Control as a false level of 4μs. duration. ITCS/ is switched in Central Control and arrives in I/O as I24D which SETS SC = 4. Refer to Figures II-7 and II-8.

SC = 4 · I24S · EXNF

I/O Control remains in SC = 4 for 4μs. or until ITCL goes false. During this period of time, IB[P => 1] is loaded with Information from the DTCU.

IB[A => 1] which contains the Buffer number plus type of Adapter Information, is transferred to the Buffer Number Field of the Result Descriptor D[35 => 31].

The DTTU number which has been temporarily stored in D[35 => 31] is transferred to its original bit position D[40 => 36]. When ITCL goes false, I24S will go true and, with EXNF ON, SETS SC = 6.

SC = 6 · D24F/

IBBF now contains the status of the Abnormal bit (ABC) and, if the Buffer was in fact Abnormal (DB1F = 1), EXNF is RESET to remember this condition.

The Character Counter is allowed to count from CC = 0 to CC = 5 during which time the Result Descriptor is formed to reflect the status of

the Buffer to be written.

CC = 1 - RESET D18F and SET D20F if the Buffer was found Not-Ready.

CC = 3 - SET D20F if the Buffer was Busy. SET D21F Read-Ready when a Write was attempted.

CC = 4 - Terminate the Write operation if the Buffer was found Busy, Not-Ready or Not-Write-Ready.

If EXNF had been RESET due to an Abnormal condition, D25F is SET in the Result Descriptor.

The Character Counter will be counted to CC = 5 only if the Write operation can proceed. With CC = 5 · D24F/ (Write), the Sequence Counter is SET to SC = 9.

SC = 9

The "W" Register and the Character Counter are cleared. MANF is SET with the first Clock pulse to indicate that this I/O Control wishes to Access the Memory Address specified by the 15 Low Order bits of the "D" Register.

At MT0D time, a Memory Read Cycle is initiated and at MT2D time, the Memory Access Obtained Flip-flop is SET with the next Clock pulse.

MISD (Memory Information Strobe Driver) finds MANF and MAOF SET and transfers MIR to the "W" Register. The Sequence Counter is incremented to 10.

SC = 10

The first Clock pulse at SC = 10 finds the Character Counter cleared. Therefore, Character 0 is transferred into the "OB" Register at the same time. The Sequence Counter is SET to 8 and the Character Counter is counted plus 1 to point to the next character to be transferred into the "OB" Register.

SC = 8 · WIRL

I/O Control waits in SC = 8 until the DTCU accepts the character being presented and requests the next character with Inquiry Time For Character Level, ITCL, (I24D). I24D causes STRF to be SET. STRF and a Clock pulse causes the character pointed to by the Character Counter to be gated in the "OB" Register. The process of transferring a character at a time to the DTCU continues until one of the following conditions occur:

1. STRF · HOLF · (CC = 0) · D17F/ - A complete word (8 characters) has been written. A Memory Cycle is necessary to refill the "W" Register.

2. STRF · HOLF · GPMS - A Group Mark Character has been sensed. End Write Transfer.

3. STRF/ · GPMS LPPF - First character is Group Mark or Buffer Final Address (I23D) has been sensed. End Write Transfer in either case.

WRITE TRANSFER DTCU

P = 2 · Q = 0 1

Refer to Figure II-12, Page 1 of 2.

With the "A" Register empty (AQF = 0) and the presence of Write Level (WIRL) from I/O Control, an A-Clock is produced which fires both ATDM and BTDM. The character from I/O Control now present on the INnL lines, is loaded into the "A" Register and AQF is turned ON. BTDM produces ITCS which signals I/O Control that a character has been received and another character is required.

The 4μs. period when ATDM and BTDM are both ON is used to enable the Translator Logics depending upon the value of the "T" Register.

P = 2 · DTT = 1 · BQ = 0 · DQ = 0

Refer to Figure II-12, Page 2 of 2.

With the character in the "A" Register (AQF = 1), Write Level (WIRL) and the 4μs. translation period past (ATDM = 0); a B-Clock is produced. The translated character (if translation was specified) is loaded into the "B" Register, BQF is turned ON, and AQF is RESET. If the character in the "A" Register is a Group Mark (A = 111111) and the Ignore Group Mark Character Flip-flop is OFF (IGM = 0), Q1F is turned ON in preparation for termination of Write Transfer. If the character in the "A" Register is NOT a Group Mark and AQF/, an A-Clock is produced which loads the "A" Register with the next character from I/O Control.

P = 2 · DTT = 1 · BQ = 1 · DQ = 0

The DTCU generates Write Level for the DTTU and waits for Terminal Character Time Level (TCTL) from the DTTU as a signal that the character has been stored in the DTTU Buffer and another character is needed. TCTL produces another B-Clock which loads the "B" Register with the next character for the DTTU.

The sequence of events which occur in the DTCU during a Write Transfer may be summarized as follows:

1. A character is received from I/O Control and loaded into the "A" Register.

2. A 4μs. Translation period follows after which time the character is transferred to the "B" Register.

3. I/O Control is informed that the "A" Register is Ready to be loaded with the next character.

4. The DTCU waits for the DTTU to accept the character now contained in the "B" Register.
5. When the DTTU has written the character into Buffer Memory, the "B" Register is loaded with the next character and the DTCU again waits for a DTTU Memory Cycle.

This process continues until either of the following conditions occur:

1. GROUP MARK CHARACTER
2. P = 2 · DTT = 1 · BQ = 0 · DQ = 0

When a Group Mark is detected in the "A" Register and Group Mark Ending is specified in the Data Communication Write Descriptor, Q1F is turned ON at B-Clock time as the Group Mark Character is transferred to the "B" Register.

P = 2 · DTT = 1 · BQ = 1 · DQ = 0

The TCTL from DTTU that is generated as a result of storing the Group Mark Character in Buffer Memory generates a B-Clock which SETS Q = 3, removes Write Level (WIRL) and RESETS BQF.

P = 2 · Q = 3

Refer to Figure II-12, Page 1 of 2.

With AQ = 0 (indicating that DTCU is through), BQ = 0 (indicating that the DTTU is through), BTD = 0 (B-Time Delay Multi has timed out), and WR = 0 (DTTU has changed states); a Final A-Clock is produced which RESETS the "P" and "Q" Registers, thus terminating the Write Transfer.

FULL BUFFER LEVEL

P = 2 · DTT = 1 · BQ = 1 · DQ = 0

Refer to Figure II-12, Page 2 of 2.

A Full Buffer Level is given by the DTTU when the next to last character position of a Buffer is being addressed. The TCTL from DTTU that is generated as a result of storing the next to last character position, generates a B-Clock which SETS Q = 2 and loads the "B" Register with the last character for the DTTU.

P = 2 · Q = 2

Refer to Figure II-12, Page 1 of 2.

An A-Clock is produced which SETS Q = 3. The "A" Register is also loaded with the next character from the System although this character will not be sent to the DTTU. Interrupt Final Address (IFAL) is sent to I/O Control at this time, thus releasing the System from Write Transfer.

Functional Detail

P = 2 · DTT = 1 · BQ = 1 · DQ = 0

The TCTL from DTTU that is generated as a result of storing the Final Character, generates a B-Clock that RESETS AQF and BQF.

P = 2 · Q = 3

With AQ = 0 (indicating that DTCU is through), BQ = 0 (indicating that DTTU is through), BTD = 0 (B-Time Delay Multi has timed out) and WR = 0 (DTTU has changed states); a Final A-Clock is produced which RESETS the "P" and "Q" Registers, thus terminating Write Transfer.

WRITE UNCERTAINTY

A unique timing situation arises if the System Write Level (WIRL) re-appears (after a B5500 Memory Cycle) at the same time that the DTTU requests another character from the DTCU with Terminal Character Time Level (TCTL). Refer to Figure II-6, Write Transfer Timing Diagram.

The result is a B-Clock during ATDM period thus reducing the necessary 4μs. Character Translation Time.

The DQF Flip-flop is used to flag this condition and provide an additional delay in which to re-translate the doubtful character.

P = 2 · Q = 0 + 1

Refer to Figure II-12, Page 1 of 2.

With the "A" Register empty (AQ = 0) and System Write Level (WIN = 1); an A-Clock is produced which fires ATDM and loads the "A" Register with the character from I/O Control. AQF is turned ON to mark the "A" Register Occupied and BTDM is fired.

P = 2 · DTT = 1 · BQ = 1 · DQ = 0

If the DTTU requests the next character at this time with TCTL, a B-Clock is produced which transfers the character from the "A" to "B". However, if the A-Time Delay Multi has not timed out (ATD = 1) when the B-Clock is fired, it is apparent that 4μs. was not allotted for translation and DQF is turned ON to flag this condition.

P = 2 · DTT = 1 · DQ = 1

With DQF ON, another translation period is allowed after which time the B-Clock is fired again and the character with the "uncertain" translation period is again transferred to the "B" Register where it is made available to the DTTU. DQF is RESET and the Normal Write Transfer resumes.

DTTU RECEIVES INFORMATION CHARACTERS

KCCS · AAN = 0 · WIN = 1 · K = 6 + 7

Refer to Figure II-13.

The DTTU prepares to receive Information characters when Write Level (WIN = 1) from DTCU goes true. SET K = 6 · M = 2, transfer the "T" to the "S" Register and initiate a Read Access on the Add Cell.

K = 6 · M = 2 · N = 6 7

Refer to Figure II-16.

Read the contents of the Add Cell into the "D" Register. If this is the first character to be stored into the Buffer (D Address Bits = 0), initiate the Address Registers by transferring "S" to the "Y" Register and turning X2F ON. If this is not the first character to be stored as would be the case if Write Transfer had been interrupted (D Address Bits ≠ 0), transfer the Address bits from the "D" Register to the "X", "Y" and "Z" Register. Load the character from DTCU into the "DA" or "DB" Register as specified by the state of DA1F. Unconditionally SET K = 7 . M = 1 where the character will be stored into Buffer Memory.

K = 7 · M = 1 · N = 6 + 7

Refer to Figure II-18.

Initiate a Memory Cycle to store the character into Buffer Memory. Terminal Character Time Level (TCTL) is generated as the character is stored and is used to signal the DTCU that the next character is required. The "X", "Y" and "Z" Registers are adjusted to address the next character location.

Write Transfer continues in this manner until one of the following conditions occurs:

1. GM - A Group Mark Character is detected and a Group Mark Ending was specified in the Write Descriptor as reflected in N = 6.
2. BFL - Buffer Final Address has been reached.
3. AAN = 1 - Some Adapter Requires Attention.
   or
   WIR = 0 - System Memory Cycle.

In the event of AAN = 1 or WIR = 0, the DTTU updates the Add Cell with the present "X", "Y", "Z" settings to indicate where Write Transfer was interrupted. Write Transfer resumes from this point after the Adapter requiring Attention has been serviced or the B5500 Memory Cycle is complete.

Functional Detail

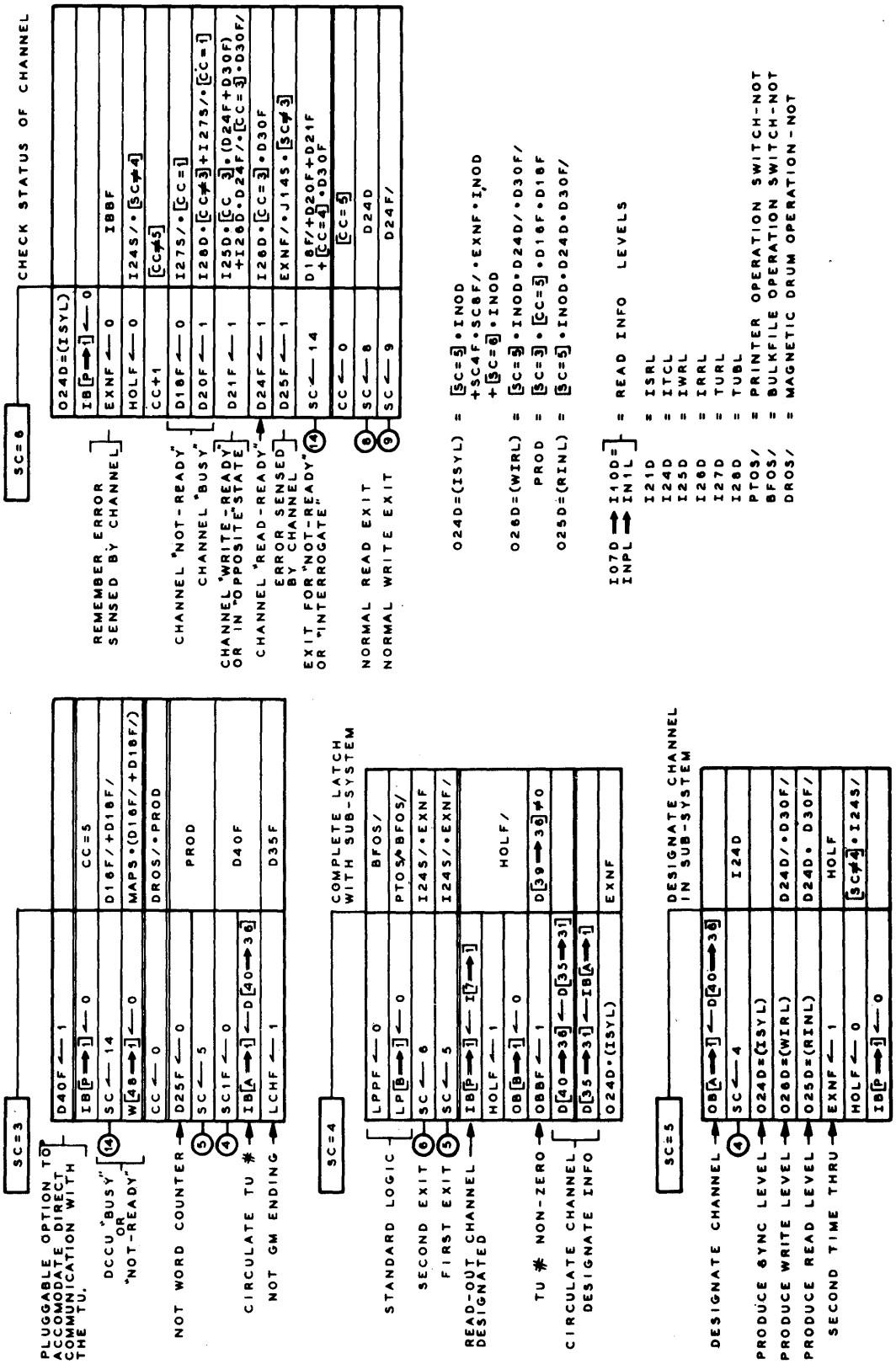


FIGURE II-7
DATA COMMUNICATION - I/O CONTROL UNIT - 1

Functional Detail

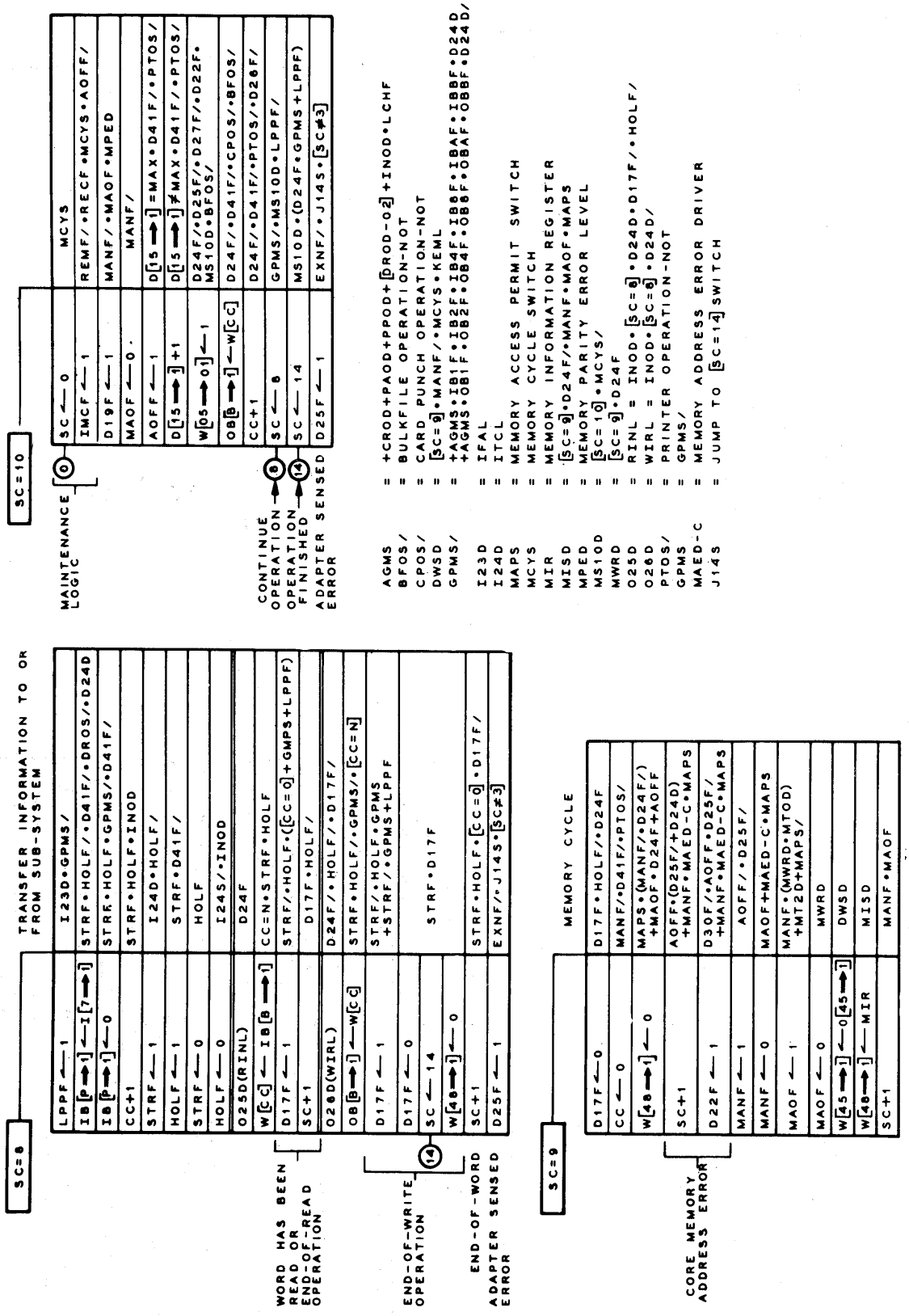


FIGURE II-8
DATA COMMUNICATION - I/O CONTROL UNIT - 2

Functional Detail

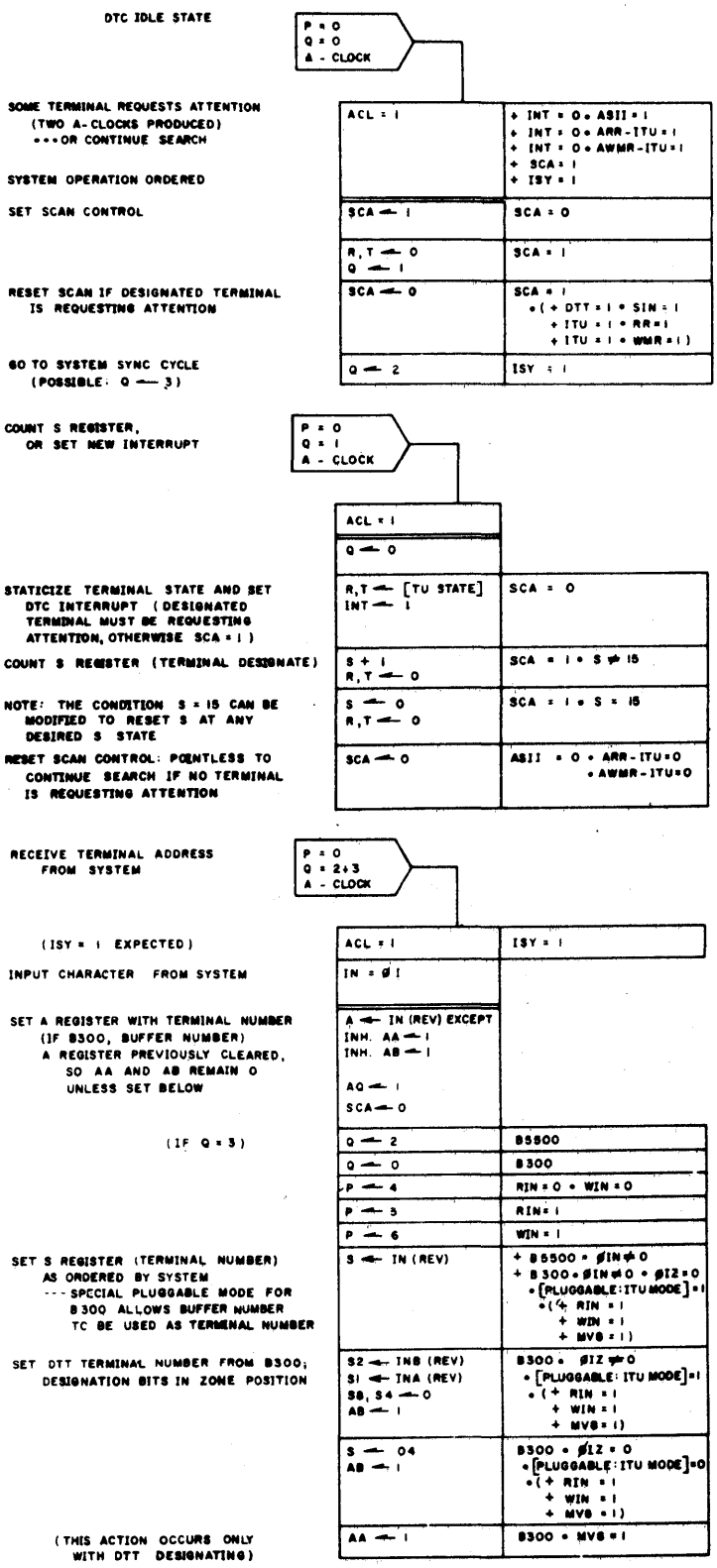


FIGURE II-9
SCAN - BEGIN SYNC (P = 0)

Functional Detail

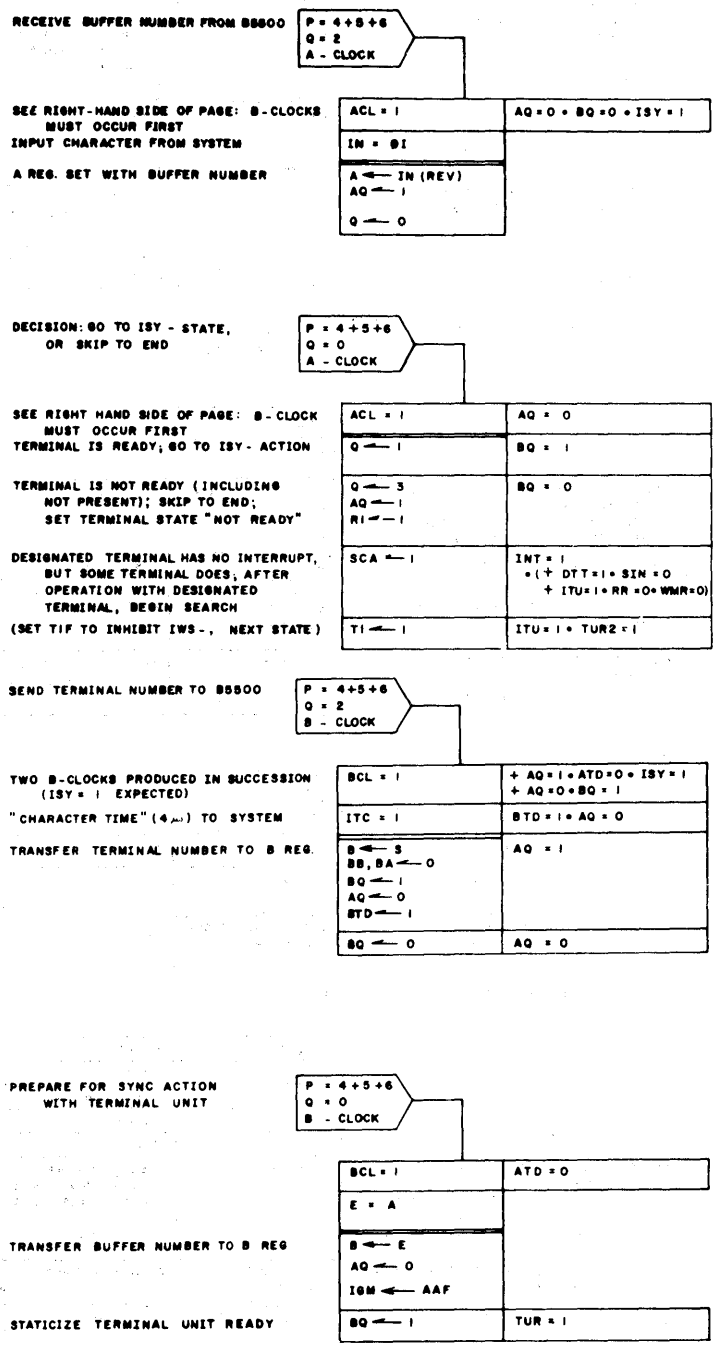


FIGURE II-10 (Page 1 of 2)
SYNC CYCLE (P = 4 + 5 + 6)

Functional Detail

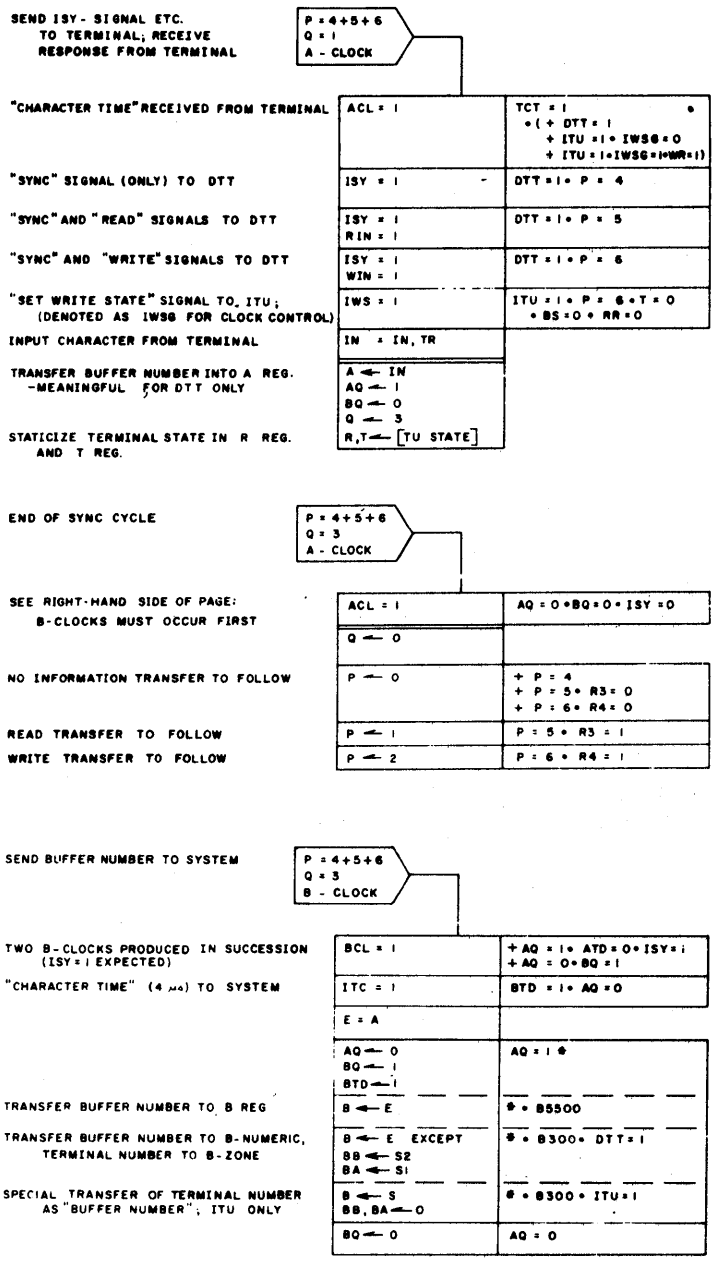


FIGURE II-10 (Page 2 of 2)
SYNC CYCLE (P = 4 + 5 + 6)

Functional Detail

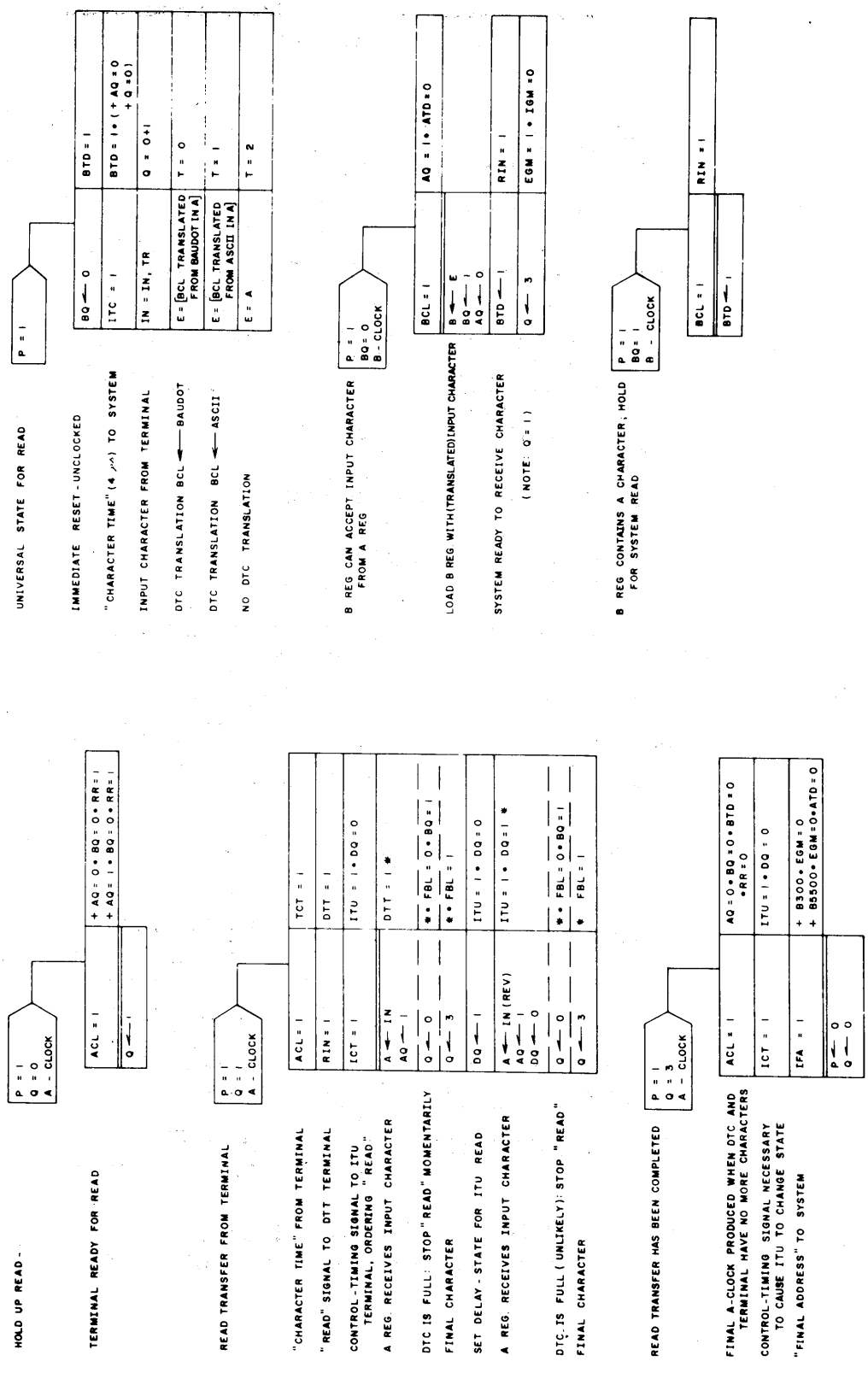


FIGURE II-11
READ (P = 1)

Functional Detail

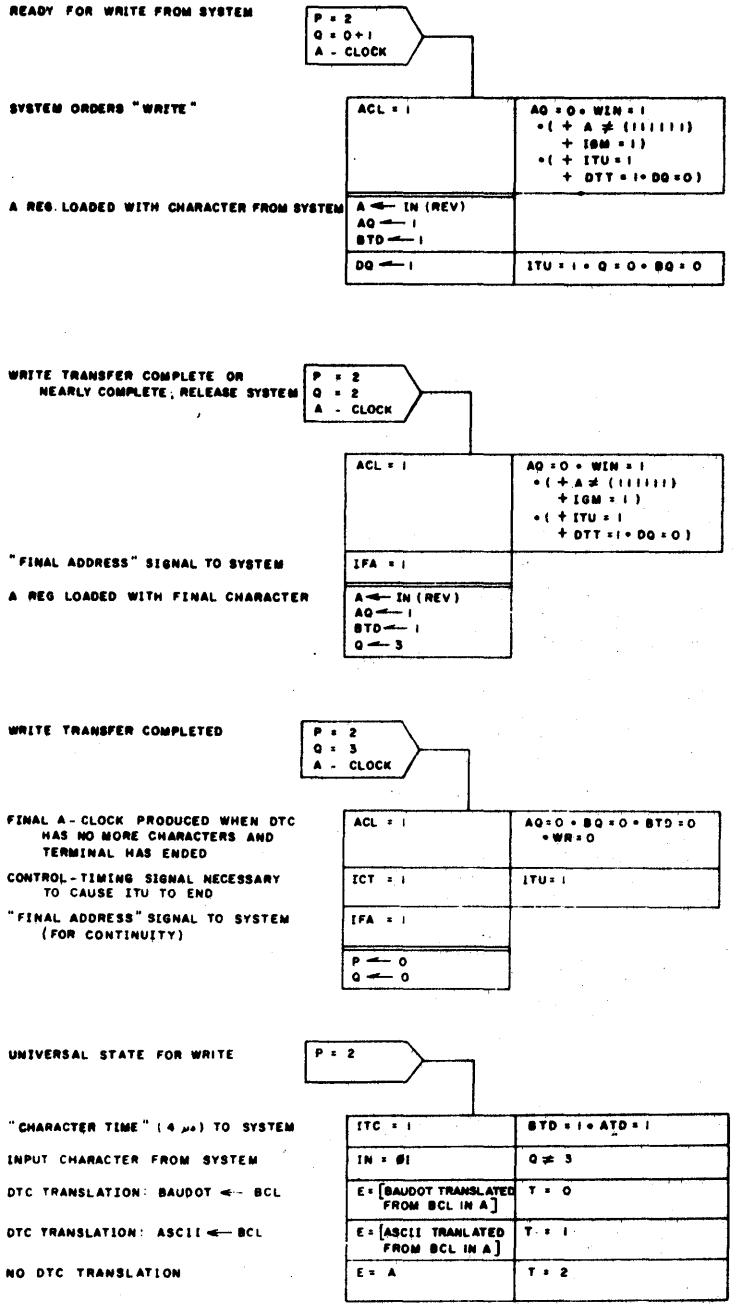


FIGURE II-12 (Page 1 of 2)
WRITE (P = 2)

Functional Detail

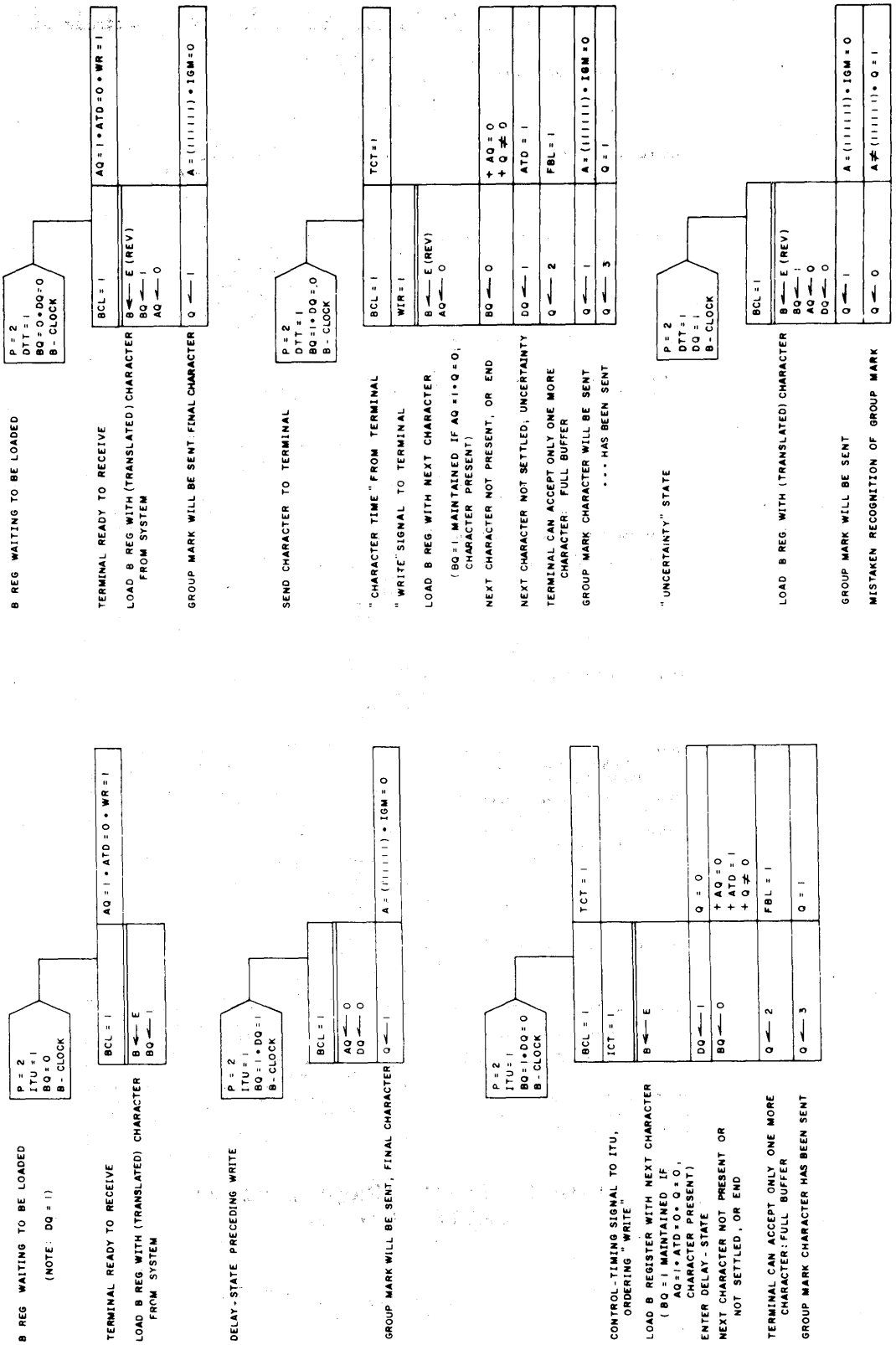


FIGURE II-12 (Page 2 of 2)
WRITE (P = 2)

Functional Detail

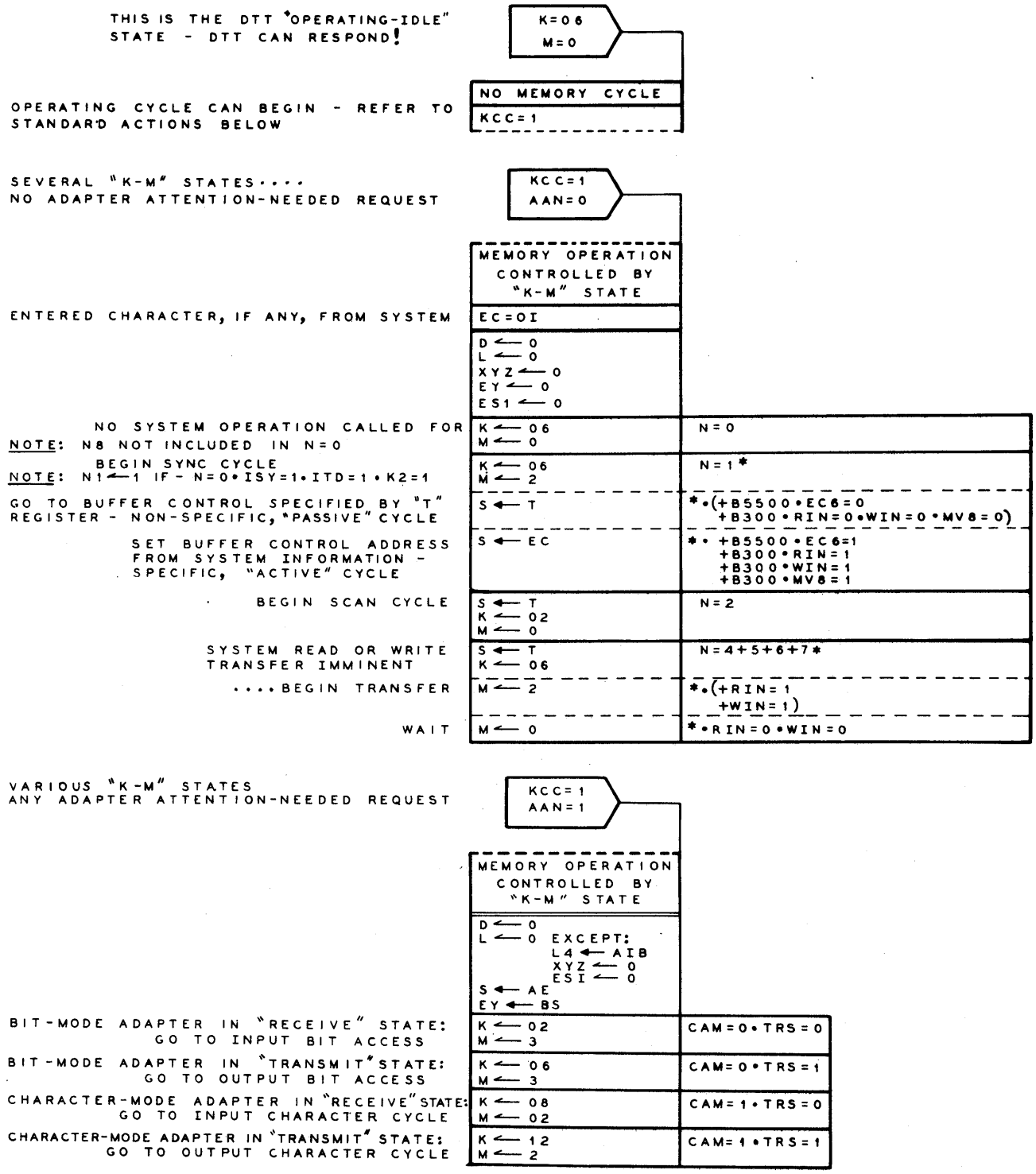


FIGURE II-13
KCCS - IDLE/SCAN FLOW CHART

Functional Detail

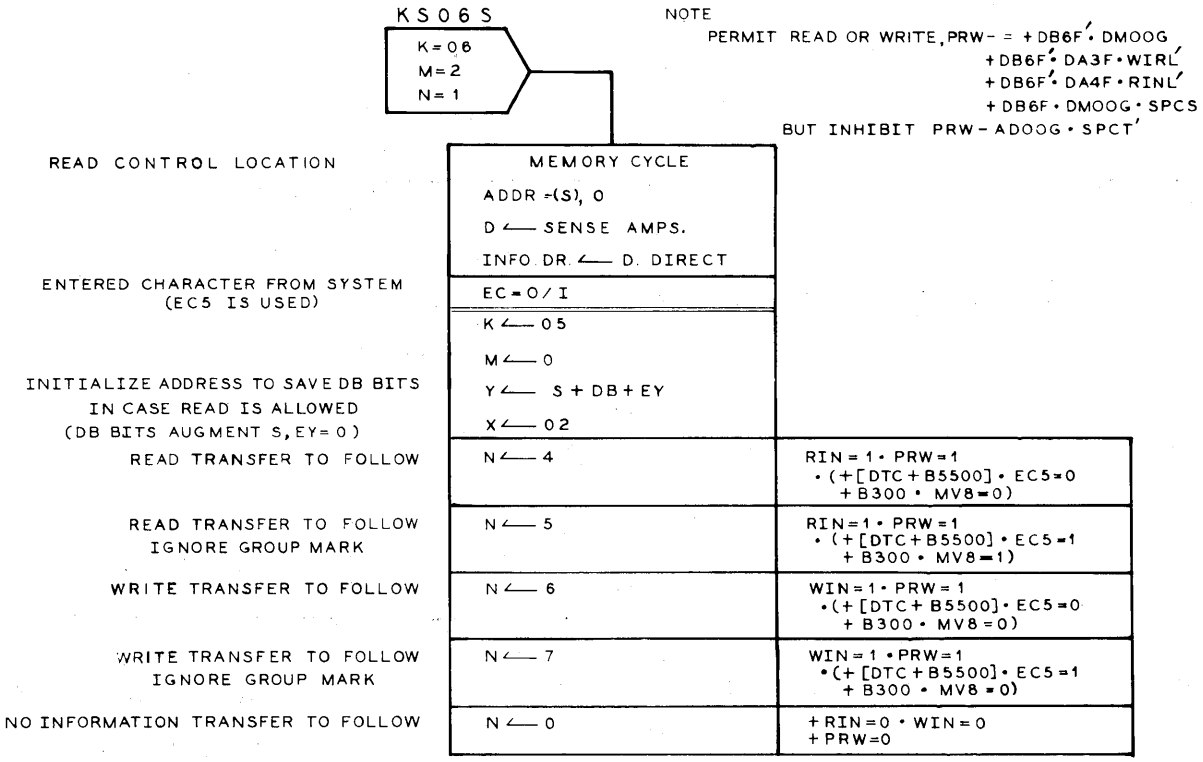


FIGURE II-14
BEGIN SYSTEM CYCLE - SYNC

Functional Detail

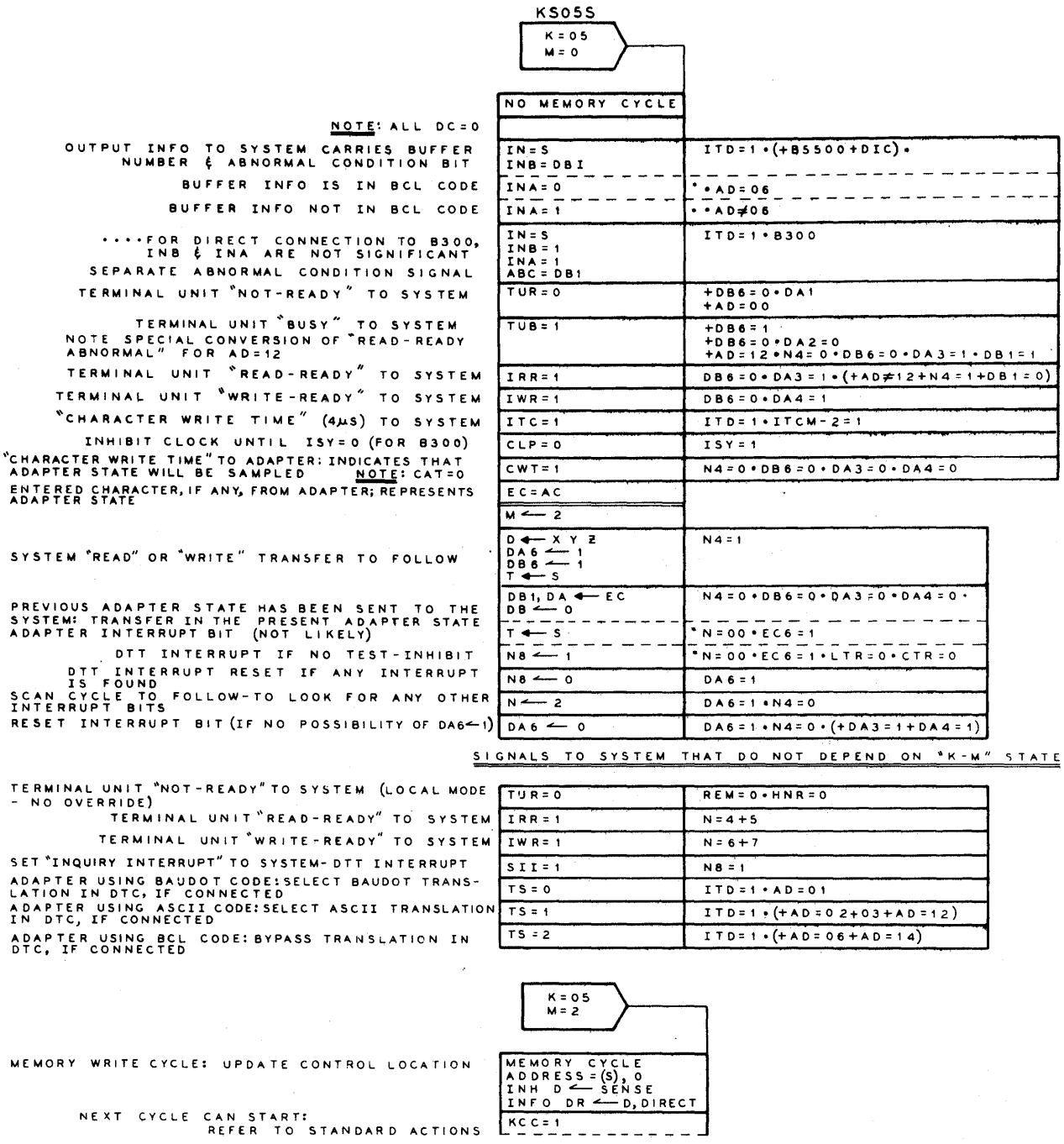


FIGURE II-15
SYNC CYCLE

Functional Detail

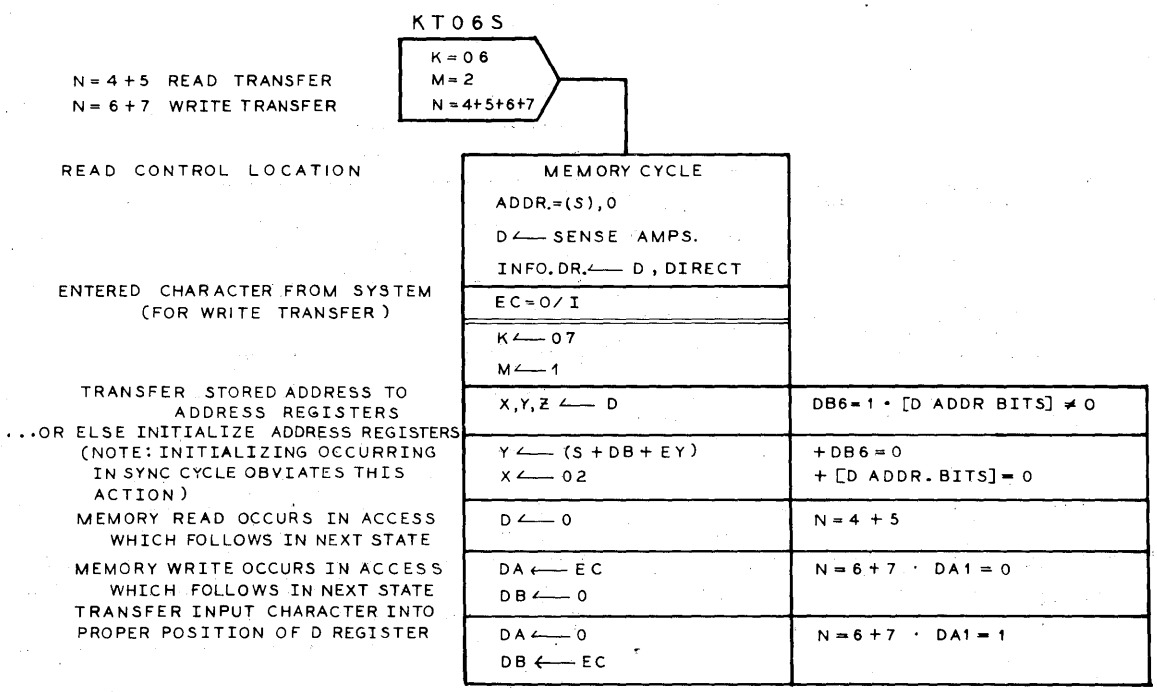


FIGURE II-16
BEGIN SYSTEM CYCLE - READ/WRITE

Functional Detail

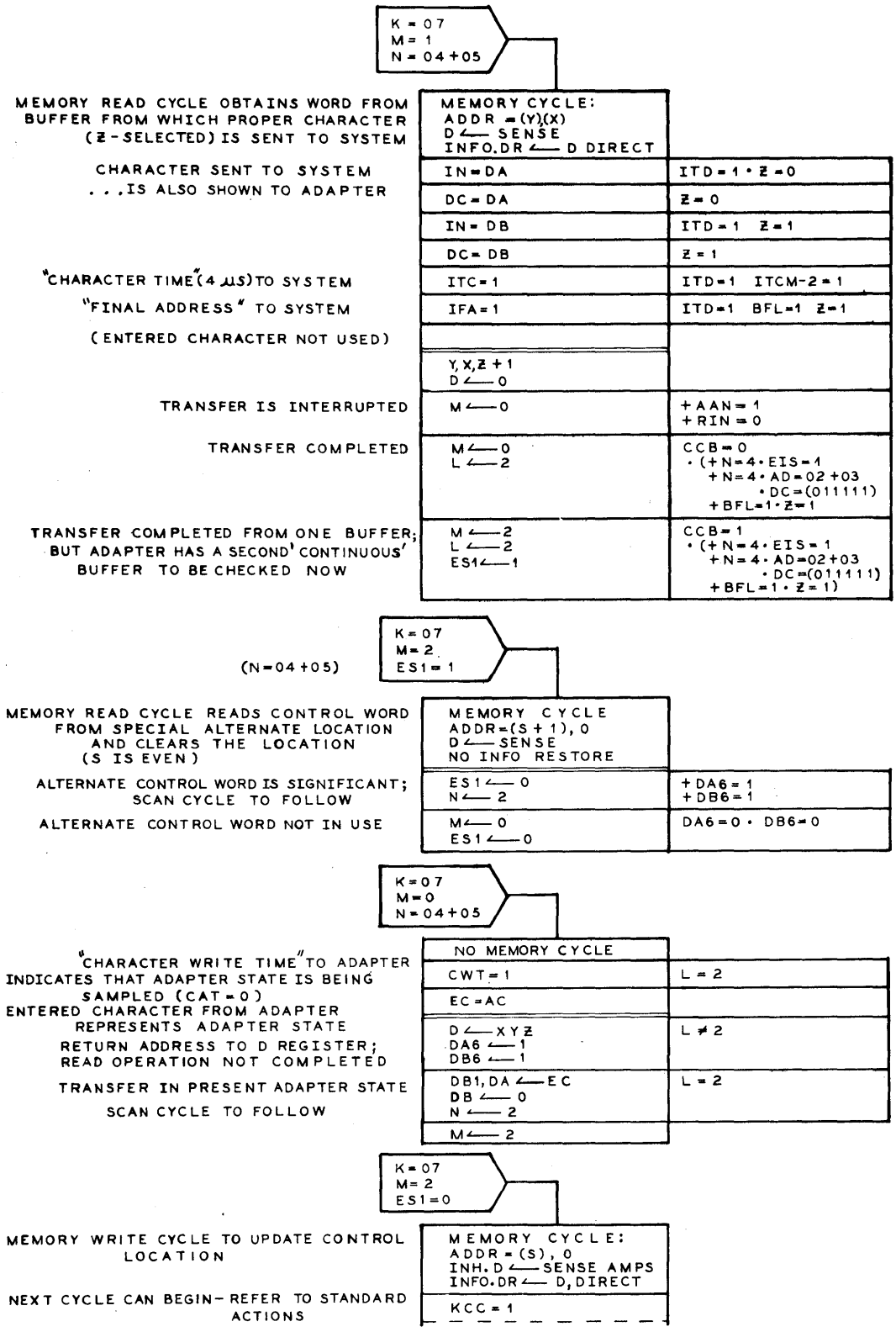


FIGURE II-17
READ TRANSFER TO SYSTEM

Functional Detail

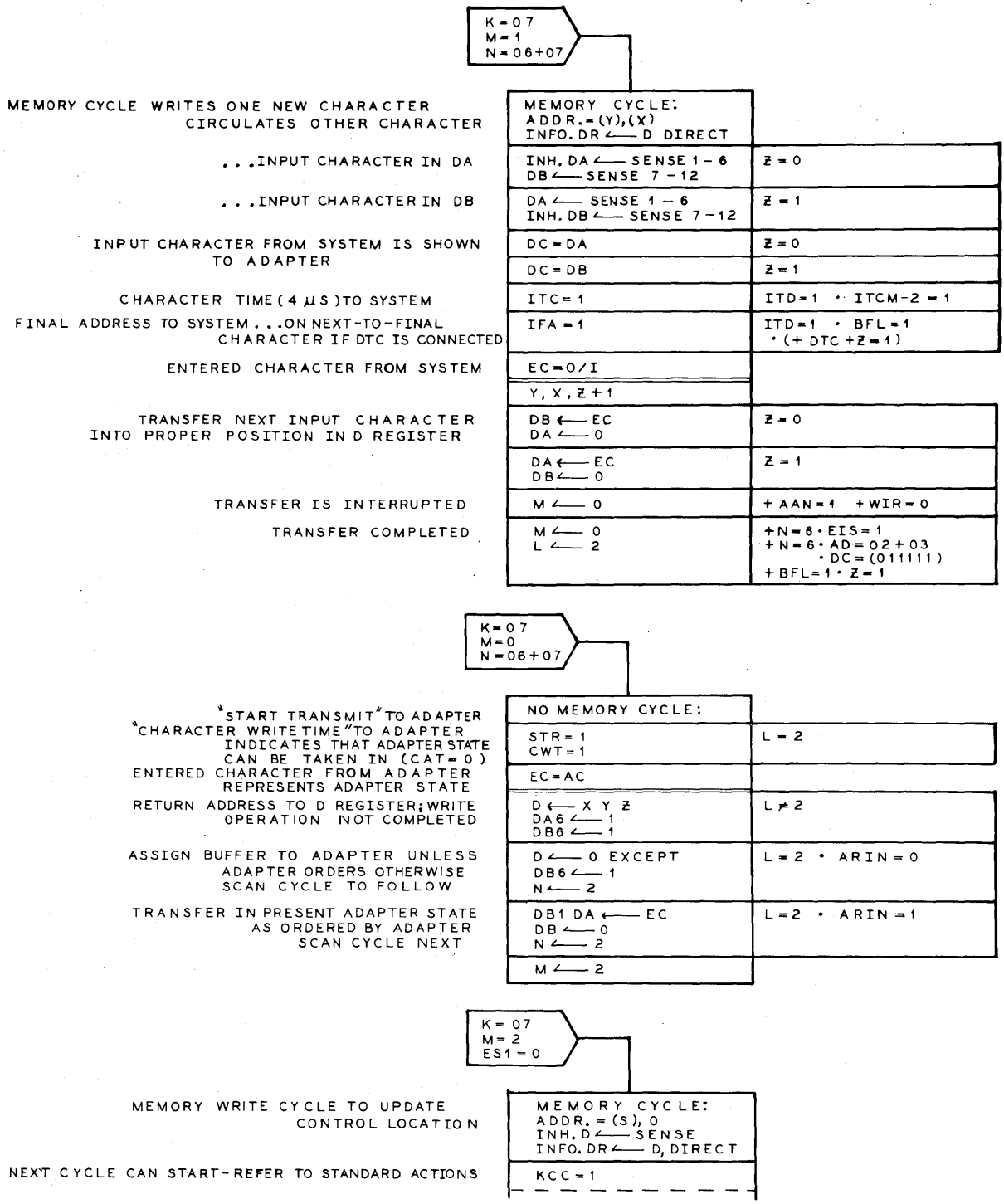


FIGURE II-18
WRITE TRANSFER FROM SYSTEM

B300 PASSIVE INTERROGATE

The Passive Interrogate informs the B300 that an Interrupt has occurred and which DTTU and Buffer initiated the Interrupt.

B300 INSTRUCTION

OP = 35 = L

M = 1 = Denotes Passive Interrogate.

N = N/A

AAA = Branch to any Interrupt except Write-Ready.

BBB = Points to DTTU Buffer number storage location.

CCC = Branch to an Interrupt Write-Ready.

When the Interrupt Flip-flop (INTF) in the B249 is not SET, the B300 Passive Interrogate will fall through to the next instruction in sequence.

The Interrupt Flip-flop in the B249 being ON, will cause the number of the DTTU and Buffer to be stored in the location pointed to by the BBB Address of the B300 Interrogate. The AAA or CCC Branch will then be taken depending on the reason for the Interrupt. The CCC Branch will be taken when the DTTU Buffer causing the Interrupt is Write-Ready. The AAA Branch will be taken when the DTTU Buffer causing the Interrupt is NOT Write-Ready. That is, the Interrupt is Read-Ready, Idle, or Busy.

GENERAL

Refer to Figure II-19.

The Passive Interrogate is initiated by the B300. The "N" Variant is read and placed in the SCF but is of no significance. The "M" Variant which must be one, is read and placed in the MVFs. The B300 now sends a Sync Level (ISYL) to the B249 while idling at CUF = 1 and MC3F with its Clock under control of the B249.

The DTCU (B249) receiving ISYL, moves from the Idle State (P = 0 · Q = 0) to begin Sync (P = 0 · Q = 2 + 3) which has no real significance during the Passive Interrogate. From this point, the DTCU goes to P4F · Q = 0 to check the DTTU (B487) for the Ready State (Power ON · Remote). If the DTTU is Ready, the DTCU goes to P4F · Q = 1 to Sync with the DTTU. However, if the DTTU is Not-Ready, the DTCU will bypass P4F · Q = 1 and will go directly to P4F · QS3S.

With the DTTU Ready, the DTCU goes to P4F · Q = 1 where it sends the Sync Level (ISYL) to the DTTU and turns Clock Control over to the DTTU.

The DTTU (B487) receiving ISYL will move from its Idle State (KCCS) to

Functional Detail

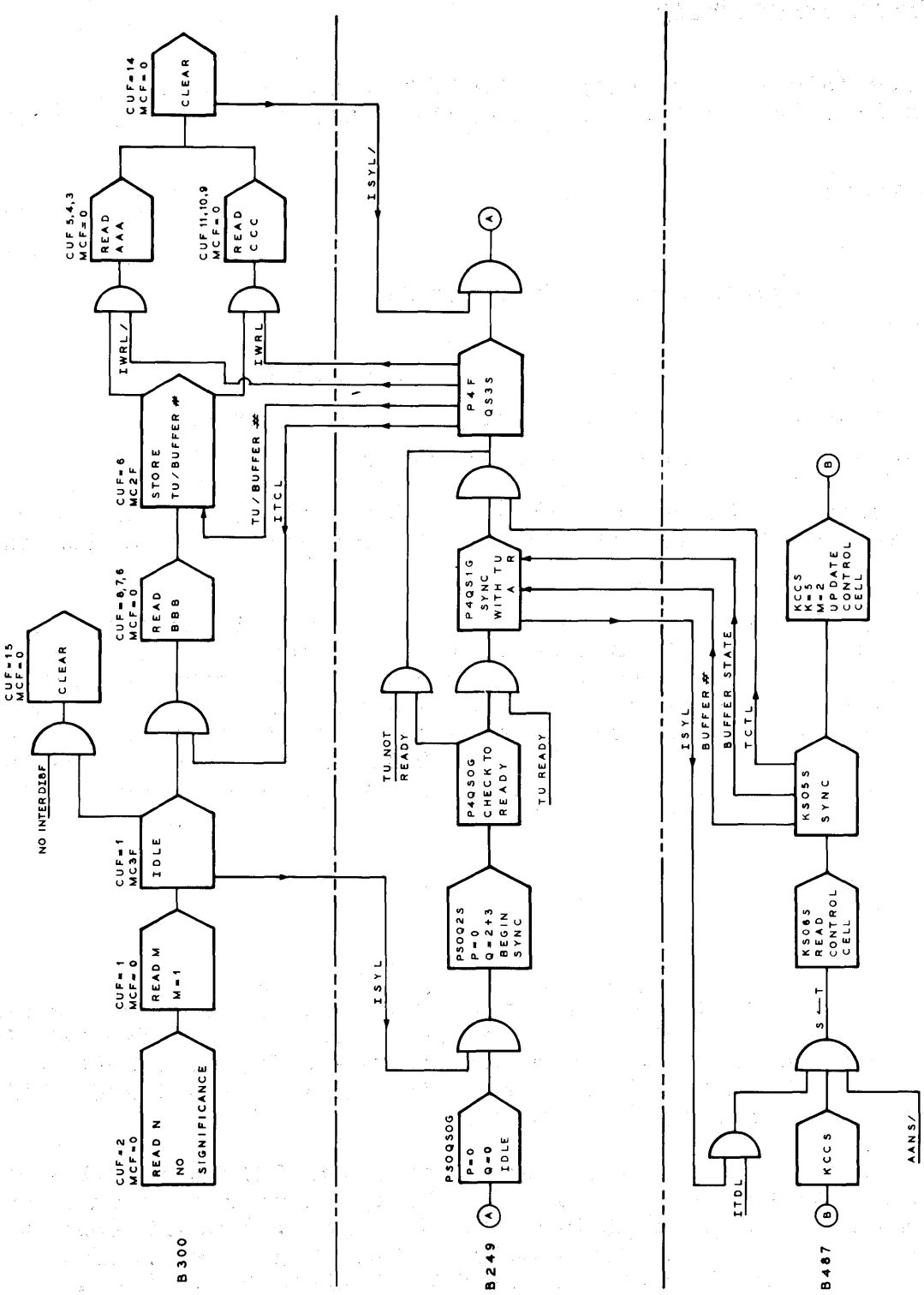


FIGURE II-19
PASSIVE INTERROGATE - BLOCK FLOW

KS06S where the Control Cell of the Buffer causing the Interrupt is read. From KS06S, the DTTU goes to KS05S where it sends the number and status of the Buffer causing the Interrupt along with a Timing pulse (TCTL) to the DTCU. The Terminal remains at KS05S for one Clock period, and then returns to KCCS. One DTTU Clock period (10μs.) is sufficient time for the DTCU to staticize the information being sent from the DTTU.

The DTCU receiving TCTL (Terminal Time for Character Level) will:

1. Place the Buffer number in the "A" Register.
2. Place the Buffer State in the "R" Register.
3. Proceed to P4F · QS3S.

At P4F · QS3S, the DTCU sends the composite DTTU Buffer number and the Buffer status to the Central Processor. In addition to this, the DTCU sends ITCL to the Central Processor starting its Clock while the DTCU turns Clock Control over to the Central Processor.

The B300 receiving ITCL starts its Clock and proceeds through CUF = 8, 7 and 6. At this time it will sample IWRL and IWRL/ (Inquiry Write-Ready and Inquiry Not-Write-Ready) to determine which Branch is to be taken.

IWRL is sent directly from R4F in the DTCU. When the Buffer causing the Interrupt is Write-Ready, IWRL will allow the B300 to go through CUF = 11, 10 and 9, resulting in the CCC Branch. When the Buffer causing the Interrupt is Not-Write-Ready (Read-Ready, Idle or Busy), IWRL/ will cause the B300 to go through CUF = 5, 4 and 3, resulting in this AAA Branch. As the B300 exits the Passive Interrogate, it sends ISYL/ to the DTCU (B249) enabling its Clock so that it may return to the Idle State, P = 0 · Q = 0.

DETAILED DESCRIPTION

CUF = 2 · MCF = 0

The "N" Variant is read and placed in the SCFs but is of no significance during the Passive Interrogate.

CUF = 1 · MCF = 0

The "M" Variant which must be 1, is read and placed in the MVFs. DI8F is SET if the Interrupt Flip-flop (INTF) in the B249 is NOT ON. This is accomplished with the term SIIL/.

CUF = 1 · MC3F

If DI8F is found ON (no Interrupt) and MV8F is OFF (not Active Interrogate), CUF is set to 15 and the instruction is complete.

Functional Detail

When an Interrupt exists, the B300 will Idle until all Card Cycles are complete (CCNL/) at which time SC7F is SET and the following actions take place:

1. Transfer SCF ("N" Variant) to CIF and then to OInLs. This action, although it occurs, is of no significance during the Passive Interrogate.

2. SET DI1F which in turn sends ISYL to the DTCU.

3. SET SYNF and clear RUNF turning Clock Control over to the DTCU.

The B300 now awaits a response from the DTCU.

B249 OPERATION

P = 0 · Q = 0 (A-Clock)

Refer to Figure II-9.

The A-Clock is enabled by ISYL arriving from the B300. When the A-Clock occurs, Q2F is SET by ISYL. It is possible that Q1F could be set if an Interrupt from some Terminal Unit occurs in concert with ISYL. However, this situation can arise only if a Central Terminal Unit (B486) is in use and the Interrupt Flip-flop was not previously set.

P = 0 · Q = 2 3 (A-Clock)

Since the B300 is still sending ISYL, an A-Clock is produced.

Most of the logic at this point is concerned with an active instruction (Active Interrogate, Read or Write). The only significant actions are to trigger ATDM (4μs.) while setting AQF, Q = 0 and P = 4. The "A" Register will receive what was in the "N" Variant of the B300 instruction, but nothing will be done with it.

P4F · Q = 0 (B-Clock)

Refer to Figure II-10, Page 1 of 2.

Before attempting to Sync with the DTTU (B487), the B249 must be certain that the DTTU has POWER ON and is in REMOTE (TURL).

ATDM will time out 4μs. after arriving at P4F · Q = 0 at which time a B-Clock is produced. If the DTTU is Ready (TUR = 1), BQF will be SET with the B-Clock. BQF will remain RESET if the DTTU is Not-Ready. AQF is unconditionally RESET.

P4F · Q = 0 (A-Clock)

When AQF is RESET, an A-Clock is ordered (ACLS). However, it cannot occur until 7μs. after the last A-Clock.

With the A-Clock, BQF which reflects the DTTU Ready status, is checked. If the DTTU was Not-Ready, BQF will be found OFF, causing AQF and RIF (DTTU Not-Ready to B300) to be SET while "Q" is set to 3. This action bypasses the Sync with the DTTU.

BQF found ON, denotes the DTTU is Ready. In this case, the only action is to SET Q = 1.

SYNC WITH DTTU

P4F · Q = 1 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

The DTCU sends ISYL to the designated DTTU and awaits a response which will come in the form of TCTL accompanying the Buffer number and State.

B487 SYNC

KCCS

Refer to Figure II-13.

ISYL arriving from the DTCU SETS "N" to 1, provided a Scan Cycle is not in progress as indicated by N = 0. With N = 1 and no Adapter requiring attention, "K" is SET to 6 if it is not already there, and "M" is SET to 2 as the Buffer number in the "T" Register is transferred to the "S" Register.

K = 6 · M = 2 (KS06S)

Refer to Figure II-14.

With Memory Addressing accomplished by "S" and "M", the Control Cell is read and held in "DA" and "DB" Since this operation is a Passive Interrogate, neither RIN (Read) or WIN (Write) is present. Therefore, the "N" Register will be cleared as "K" is SET to 5 and "M" to 0.

K = 5 · M = 0 (KS05S)

Refer to Figure II-15.

The contents of the "S" Register which points at the Buffer causing the Interrupt, along with the status of that Buffer/Adapter ("DA" and "DB") is sent to the DTCU. The term ITCL is also generated and sent to the DTCU where it becomes TCTL.

The DTTU Clock is disabled as long as ISYL is present. However, the only time this logic will have any effect is when the DTTU is direct connected to a B300. With DTCU operation, this logic has no effect because ISYL will go false prior to the 10μs. Clock period. The Timing will be the DTTU Clock pulse that SETS KS05S and triggers ITCM-1 4μs.

When ITCM-1 times out, ITCM-2 is triggered and develops the 4μs. ITCL pulse which is sent to the DTCU as TCTL. One microsecond after TCTL arrives at the DTCU, an A-Clock will occur. This A-Clock will cause ISYL to go false, enabling the DTTU Clock. Since the DTTU Clock was enabled 5μs. after it was disabled, the next Clock pulse will occur at the minimum time which is 10μs. after the last DTTU Clock pulse. When this Clock pulse occurs, the DTTU will return to KCCS.

DTCU

P4F̂ · Q = 1 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

When the DTTU sends TCTL along with the Buffer number and status, an A-Clock is produced. At this time, the following actions will occur:

1. The Buffer number is placed in the "A" Register while AQF is SET and ATDM is triggered.
2. The Buffer State is placed in the "R" Register whose significance is:
   a. R1F = DTTU Not-Ready.
   b. R2F = DTTU Busy.
   c. R3F = DTTU Read-Ready.
   d. R4F = DTTU Write-Ready.
3. BQF is RESET.
4. "Q" is SET to 3.

P4F · Q = 3

There will be two B-Clocks produced and then one A-Clock.

The first B-Clock is generated when ATDM times out, AQF is ON, and ISYL comes from the B300.

The actions of this first B-Clock are as follows:

1. Place the Buffer number from the numeric portion of the "A" Register through the Translator Encoder (no translation) to the "B" Register numerics.
2. Transfer the DTTU number from S1F and S2F to BAF and BBF respectively.
3. RESET AQF and SET BQF.
4. Trigger BTDM which in turn sends ITCL to the System after AQF

changes State. The reason for gating AQF/ into the logic to send ITCL to the Central Processor, is to provide a .5μs. delay to insure that the Information Lines (DTTU/Buffer number) have stabilized.

The B-Clock is now enabled by AQF being OFF and BQF ON. The second B-Clock will occur in the minimum time (7μs.) and its only function is to RESET BQF, disabling the B-Clock.

When the B300 has completely utilized the information being sent from the DTCU, it will return ISYL/ (CUF = 14). When this happens, the A-Clock is produced, clearing "P" and "Q" to return the DTCU to its Idle State.

B300

CUF = 1 · MC3F

Refer to Figure II-20.

ITCL arriving from the DTCU fires the Clock B.O. producing one CCP at which time the following takes place:

1. Set RUNF turning the B300 Clock back ON.
2. INnL → AIF - Place the DTTU/Buffer number in AIF.
3. CUF → 8 - Clear MC3F to read the BBB Address.

CUF = 8, 7 and 6 (MCF = 0)

Read the BBB Address and place it in MAR. At CUF = 6, the DTTU Buffer number is transferred from AIF → CIF.

CUF = 6 · MC2F

The number of the DTTU and Buffer causing the Interrupt is stored in the location pointed to by BBB (MAR Write).

The Branch to be taken is now determined by checking IWRL and IWRL/ which reflects the State of R4F in the DTCU.

With IWRL, CUF is SET to 11 and the CCC Branch is taken. With IWRL/, CUF is SET to 5 and the AAA Branch is taken.

At CUF = 14, DI1F is cleared. This sends ISYL/ to the DTCU releasing it.

Functional Detail

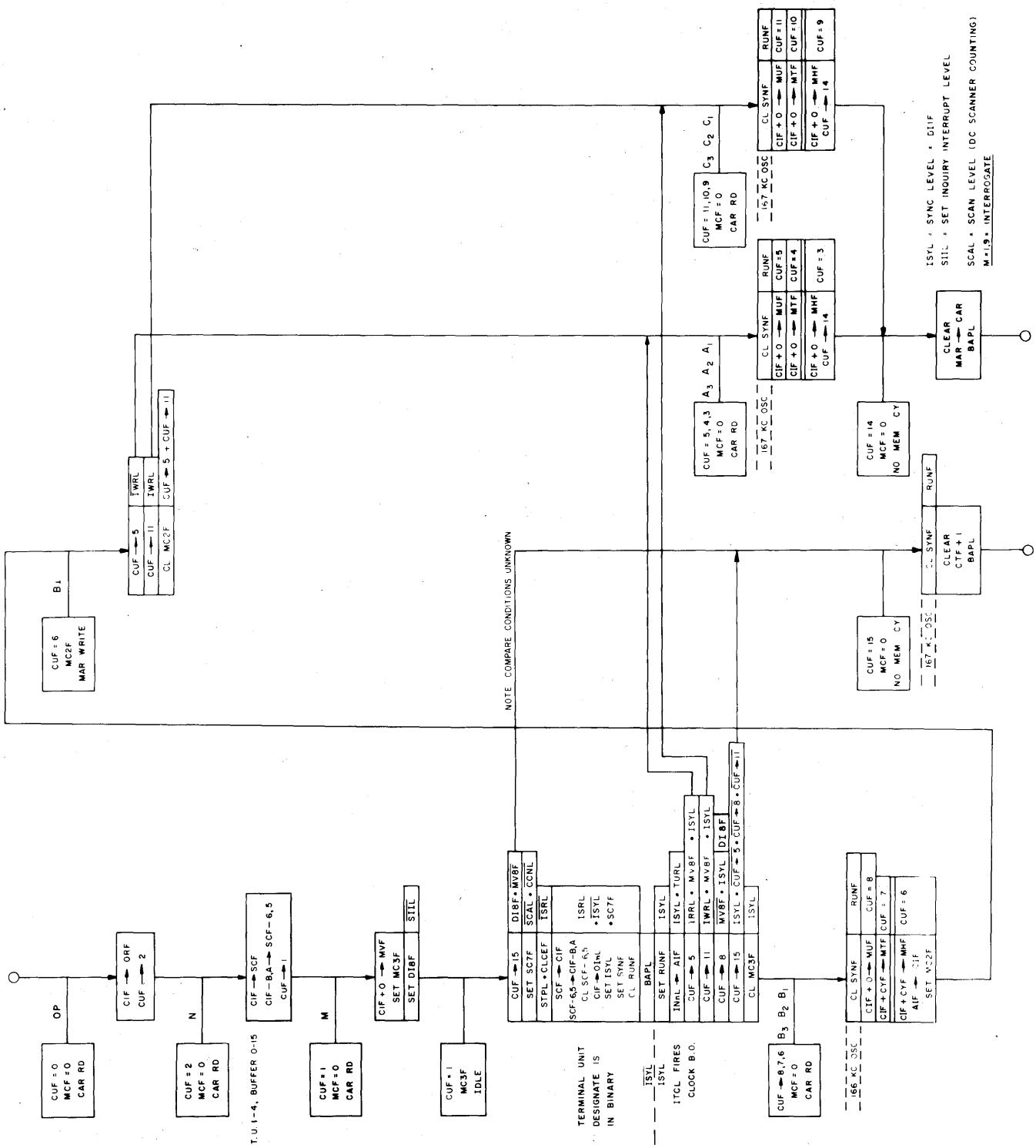


FIGURE II-20
B300 INTERROGATE FLOW

B300 ACTIVE INTERROGATE

The Active Interrogate provides the B300 with a method of checking the status of a specific Terminal Unit and Buffer/Adapter within that DTTU. Reference Figure II-21.

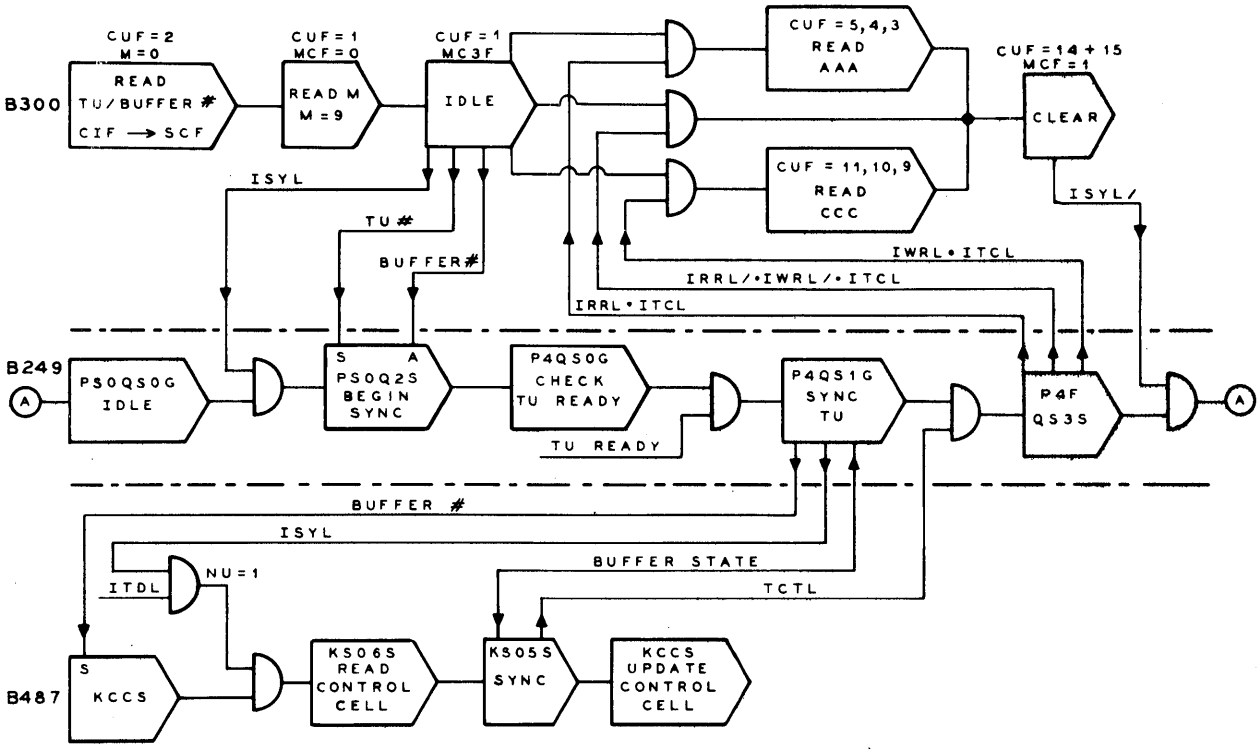


FIGURE II-21
ACTIVE INTERROGATE - BLOCK FLOW

B300 OPERATION

OP = L = 35

M = 9

N = DTTU/Buffer Designate

Zones = DTTU Number

Numeric = Buffer Number

AAA = Branch to where Buffer is Read-Ready.

BBB = N/A

CCC = Branch to where Buffer is Write-Ready.

The Active Interrogate will fall through to the next instruction in sequence when the selected Buffer is neither Read-Ready or Write-Ready.

DETAILED DESCRIPTION

CUF = 2 · MCF = 0

Refer to Figure II-20.

The "N" Variant (DTTU/Buffer number) is read and placed in the SCFs with SCF1 through 4 receiving the Buffer number and SCF5 and 6 receiving the DTTU number.

CUF = 1 · MCF = 0

The "M" Variant is read and placed in the MVFs. MV1F ON signifies Interrogate while MV8F signifies Active. Note that the 8-bit bypasses the Adder on the CIF → MVF.

CUF = 1 · MC3F

The B300 will allow BAPL until all Card Cycles are complete at which time SC7F is SET. With SC7F ON, the following actions take place:

1. SCF → CIF - Transfer the DTTU/Buffer number to the CIF and CIF → OInL and thence to the Output Information Lines.
2. SET ISYL - DI1F is SET and sends ISYL to the DTCU.
3. SET SYNF - Clear RUNF turning Clock Control over to the DTCU.

B249 DTCU

P = 0 · Q = 0 (A-Clock)

Refer to Figure II-9.

The A-Clock is enabled (ACL) by ISYL arriving from the B300. When the A-Clock pulse occurs, Q2F is SET. It is possible that Q1F could also be set if a Scan Cycle is in progress (SCA = 1).

P = 0 · Q = 2 + 3 (A-Clock)

The A-Clock remains enabled (ACL) by ISYL.

The Buffer number from the B300 is placed in the numeric portion of the "A" Register while the Zone positions are cleared. In conjunction with this, the "A" Register is marked "Occupied" by AQF being SET. The Zone bits of the DTTU/Buffer number character being sent from the B300 are placed into S1F and S2F while S4F and S8F are cleared. Note however, that the "S" Register is SET equal to 4 if the Zones are both OFF.

INAL · INBL/ - S = 1
INAL/ · INBL - S = 2
INAL · INBL - S = 3
INAL/ · INBL/ - S = 4

Since an Active Interrogate is called for, the B300 will send MV8L to the DTCU. This will cause "P" to be SET to 4 while "Q" is cleared.

P = 4 · Q = 0 (B-Clock)

Refer to Figure II-10, Page 1 of 2.

Since P = 4 · Q = 0 was entered because of an A-Clock, ATDM will be ON for 4μs. When ATDM times out, the B-Clock pulse occurs. With the B-Clock, the Buffer number is transferred to the "B" Register and AQF is RESET. The Terminal is checked for POWER ON and REMOTE (TURL) and if it is Ready, BQF is SET.

BQF remains OFF if the DTTU is Not-Ready. The DTTU must be checked for Ready at this time because P = 4 · Q = 1 depends on a Timing pulse from the DTTU. Therefore, Q = 1 must be bypassed when the DTTU is Not-Ready.

P = 4 · Q = 0 (A-Clock)

With AQF RESET, the A-Clock is enabled. When the Clock pulse occurs, the State of BQF which reflects the DTTU State is checked. With BQF ON, "Q" is SET to 1 to Sync with the DTTU. With BQF OFF, "Q" is SET to 3 to Sync with the System. R1F is SET to send the Not-Ready condition to System and AQF is SET.

The Scan Flip-flop (SCAF) will be SET if the Interrupt Flip-flop is ON and the selected DTTU does not have its Interrupt Flip-flop (N8F) ON as reflected by SIN = 0. This will allow the DTCU to scan for the DTTU that caused INTF to be ON after the Interrogate is complete.

P = 4 · Q = 1 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

With P = 4, ISYL and MV8L are sent to the B487. Along with this, the Buffer number held in the "B" Register is also sent to the DTTU.

The B249 now awaits a response from the Terminal Unit.

DTTU (B487) SYNC

N1F is SET by ISYS. Note that this is Floating logic and can occur on most "K" settings.

KCCS

Refer to Figure II-13.

When no Adapter requires attention (AANS/), the following will take place:

1. SECS - The Buffer number is gated through the EC (Entrance Char-

acter) Switches and placed in the "S" Register so that it can be used for Addressing. This is accomplished by B300 connection and MV8L.

2. "K" is SET to 6 and "M" is SET to 2.

K = 6 · M = 2: SYSTEM ADDRESS ACCESS (SYNC)

Refer to Figure II-14.

The contents of the ADD (Control) Cell are read and placed in "DA" and "DB".

Since the DTCU is not sending RINL or WINL, the "N" Register is cleared as "K" is SET to 5 and "M" is SET to 0.

K = 5 · M = 0 (KS05S)

Refer to Figure II-15.

The Buffer number as contained in the "S" Register is sent to the DTCU but is of no significance.

The status of the Buffer is sent to the DTCU from the "DA" and "DB" Registers with the following significance:

1. DA1F = Buffer Not-Ready (TUR = 0).
2. DA2F = Buffer Busy (TUB = 1).
3. CA3F = Buffer Read-Ready (IRR = 1).
4. DA4F = Buffer Write-Ready (IWR = 1).
5. DB6F = Buffer Busy (TUB = 1).

ITCS (Inquiry Time for Character Switch) is generated 4μs. after Clock time and is sent to the DTCU where it becomes TCTS.

The DTCU will staticize the Buffer status and the Buffer type approximately 1μs. after TCTS arrives. At this time, the DTCU sends ISYL/ to the Terminal.

Since ISYL/ arrives at the Terminal approximately 5μs. after the last Clock pulse, the DTTU Clock will continue to run.

The Sync between the DTCU and the DTTU is now complete. The DTTU will return to KCCS with "N" equal to 0 or 2 depending on the Interrupt (DA6F) condition of the interrogated Buffer.

B249

P = 4 · Q = 1 (A-Clock)

Functional Detail

Refer to Figure II-10, Page 2 of 2.

The DTCU has been idling at this point awaiting the DTTU response. The response will be the status of the Addressed Buffer/Adapter along with the 4μs. Timing pulse TCTS. The Buffer number will also be sent but has no significance.

When TCTS arrives, an A-Clock will occur at which time the following actions take place:

1. "R", "T" ← DTTU State - The State of the Addressed Buffer is staticized in the "R" Register where:
   a. R4F = Buffer Write-Ready.
   b. R3F = Buffer Read-Ready.
   c. R1F = Buffer Not-Ready

   The Adapter type is staticized in the "T" Register but has no significance during the Active Interrogate.
2. "A" ← IN - Place the Buffer number into the numeric portion of the "A" Register. This logic has no significance to the Active Interrogate.
3. AQF ← 1 - Mark the "A" Register "Occupied".
4. BQF ← 0 - Mark the "B" Register "Unoccupied".
5. Q2F ← 1 - Set "Q" to 3.

P = 4 · Q = 3

During Q = 3, the DTTU Buffer number and the Buffer status will be sent to the B300 where only the Buffer status will be utilized. Two B-Clocks will be produced to send this information to the Central Processor. The Processor will then return ISYL = 0 to produce one A-Clock which provides Exit logic from Q = 3.

P = 4 · Q = 3 (B-Clock)

The first BCLP occurs when ATDM times out with the logic AQF = 1 · ATD = 0 · ISY = 1. With this pulse, the Buffer number is placed in the numeric portion of the "B" Register while the DTTU number is placed in BAF and BBF. AQF is RESET and BQF is SET to mark the "B" Register "Occupied". AQF = 0 is included in this logic to provide a .5μs. delay to allow the "B" Register and Information Lines time to settle down.

The second BCLP simply clears BQF. The DTCU is now at P = 4 · Q = 3. A-Clock with AQF and BQF/ is awaiting ISY = 0 to be returned from the B300.

B300 OPERATION

CUF = 1 · MC3F

Refer to Figure II-20.

ITCL arriving at the Central Processor fires the Clock B.O. providing one CCP. The status of the DTTU is now checked for Write-Ready and Read-Ready. If the DTTU is Read-Ready, IRRL being sent from the DTCU will SET CUF to 5 and an AAA Branch is taken.

If the DTTU is Write-Ready, IWRL will SET CUF to 11 and the CCC Branch is taken. If the DTTU is neither Read-Ready nor Write-Ready, CUF will be SET to 15, completing the instruction. When the B300 completes (CUF = 14 + 15), DI1F will be cleared. This sends ISYL = 0 to the DTCU.

B249 OPERATION

P = 4 · Q = 3 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

ISY = 0 arriving from the B300, produces an A-Clock which clears the "P" and "Q" Registers thus returning the DTCU to its Idle State.

B300 DATA COMMUNICATION READ

Refer to Figures II-22 and II-24.

The Read instruction will transfer the contents of a specified Buffer in the DTTU (B487) to the DTCU (B249) where the information is translated to BCL and then sent to the B300.

The Read is initiated by the B300. The Central Processor sends a six bit character to the DTCU defining the Terminal Unit and Buffer it wishes to read. Along with this character, the B300 sends several Control Levels, the most important of which are ISYL (Sync) and RINL (Read). The DTCU places the Zone bits of that character in its "S" Register so that it points to the specified DTTU.

The numeric bits (Buffer number) are placed in the DTCU "A" Register, transferred to the "B" Register and then sent to the selected DTTU. The Sync Level (ISYL) and the Read Level (RINL) will accompany the Buffer number being sent to the DTTU.

The DTTU, recognizing the Sync and Read Control Levels, will place the number of the Buffer to be read into its "S" Register and will proceed through a Sync Cycle. As a result of the DTTU Sync, the status of the Buffer to be read and the type of Adapter are sent to the DTCU. At

Functional Detail

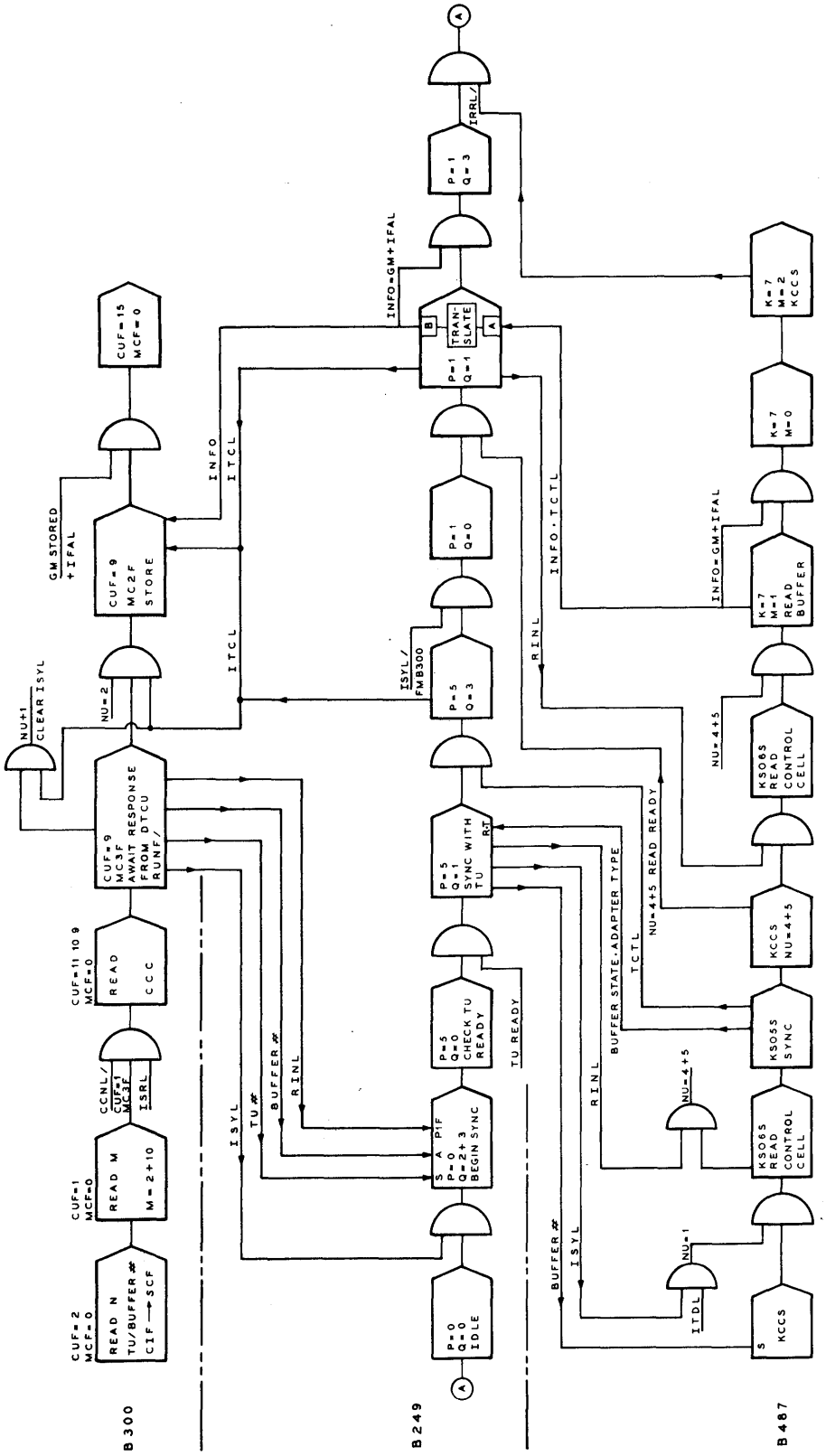


FIGURE II-22
B300 READ - BLOCK FLOW

the DTCU, this information is staticized into the "R" and "T" Registers respectively. The DTTU is released back to the Idle State (KCCS) while the DTCU passes along to the Central Processor the status of the Addressed Buffer.

The Central Processor samples the status lines to determine if the read can take place. If the Buffer can not be read, the DTCU will send IRRL/ (Inquiry Read-Ready-Not) causing the B300 to take the BBB Branch. If the DTCU returns TURL/ (DTTU Not-Ready), the B300 will take the AAA Branch. If neither of these conditions exist, the Read Transfer will take place.

The Timing for the Read is controlled by the DTTU where the information is transferred at its Clock rate (10μs. /character). Each Clock pulse in the DTTU will cause a character to be read from the Buffer and sent to the DTCU along with the 4μs. Timing pulse TCTL.

The character is placed in the DTCU "A" Register. From the "A" Register, the character is presented to the Translator whose output is placed in the "B" Register. Once this character reaches the "B" Register, the "A" Register is free to accept another character from the DTTU. Whenever a character reaches the "B" Register, a Timing pulse (ITCL) is sent to the B300 informing it that a character is on the Information Lines.

The B300, recognizing ITCL, will produce a CCP to accept the character. This process continues until a Group Mark is recognized or the Final Address Location of the Buffer being read has been reached. In either case, the three Units will be released in this order:

1. DTTU.
2. B300.
3. DTCU.

READ - DETAIL DESCRIPTION

B300

OP = L

M = 2 - Read to Group Mark.
10 - Read entire Buffer, Ignore Group Mark.

N = Terminal Unit and Buffer Designate.
Zone = DTTU Number.
Numeric = Buffer Number.

AAA = Branch on Terminal Unit Not-Ready.

BBB = Branch on Buffer Not-Read-Ready.

CCC = Input Field.

Functional Detail

The instruction will read the Buffer within the designated DTTU to the Field pointed to by CCC.

The AAA Branch will be taken if the Terminal Unit is Not-Ready (LOCAL or POWER OFF).

The BBB Branch will be taken if the designated Buffer is Busy, Write-Ready, or Not-Ready. It is permissable to read an Idle Buffer.

CUF = 2 · MCF = 0

Refer to Figure II-23.

The "N" Variant (DTTU/Buffer number) is read and placed in the SCFs with SCF1 through 4 receiving the Buffer number and SCF5 and 6 receiving the DTTU number.

CUF = 1 · MCF = 0

The "M" Variant is read and placed in the MVFs. MV2F ON, signifies Read while MV8F signifies Ignore Group Mark. Note that MV8F bypasses the Adder on the CIF → MVF transfer.

CUF = 1 · MC3F

The Processor Idles at this point to allow BAPL until all Card Cycles are complete at which time SC7F is SET. With SC7F ON and the DTCU Ready (ISRL), the Processor proceeds to CUF = 11.

Should the DTCU be found Not-Ready, ISRL/ will clear CEF.

CUF = 11, 10, 9 · MCF = 0

The CCC Address which points at the MSD of the Input area is read and placed in MAR.

At CUF = 9 · MCF = 0, the following actions take place:

1. SCF → CIF - Transfer the DTTU/Buffer number from the SCF to the CIF and CIF → OInL and thence to the Output Information Lines for routing to the DTCU. Note that the CIF → OInL is binary.

2. SET ISYL - The actual logic is SET DI1F which in turn sends ISYL (Inquiry Sync Level) to the DTCU.

3. SET SYNF - Turn Clock Control over to the DTCU.

4. Clear RUNF

5. SET RINL - The actual logic is to SET DI2F which in turn sends RINL (Read Inquiry Level) to the DTCU.

Functional Detail

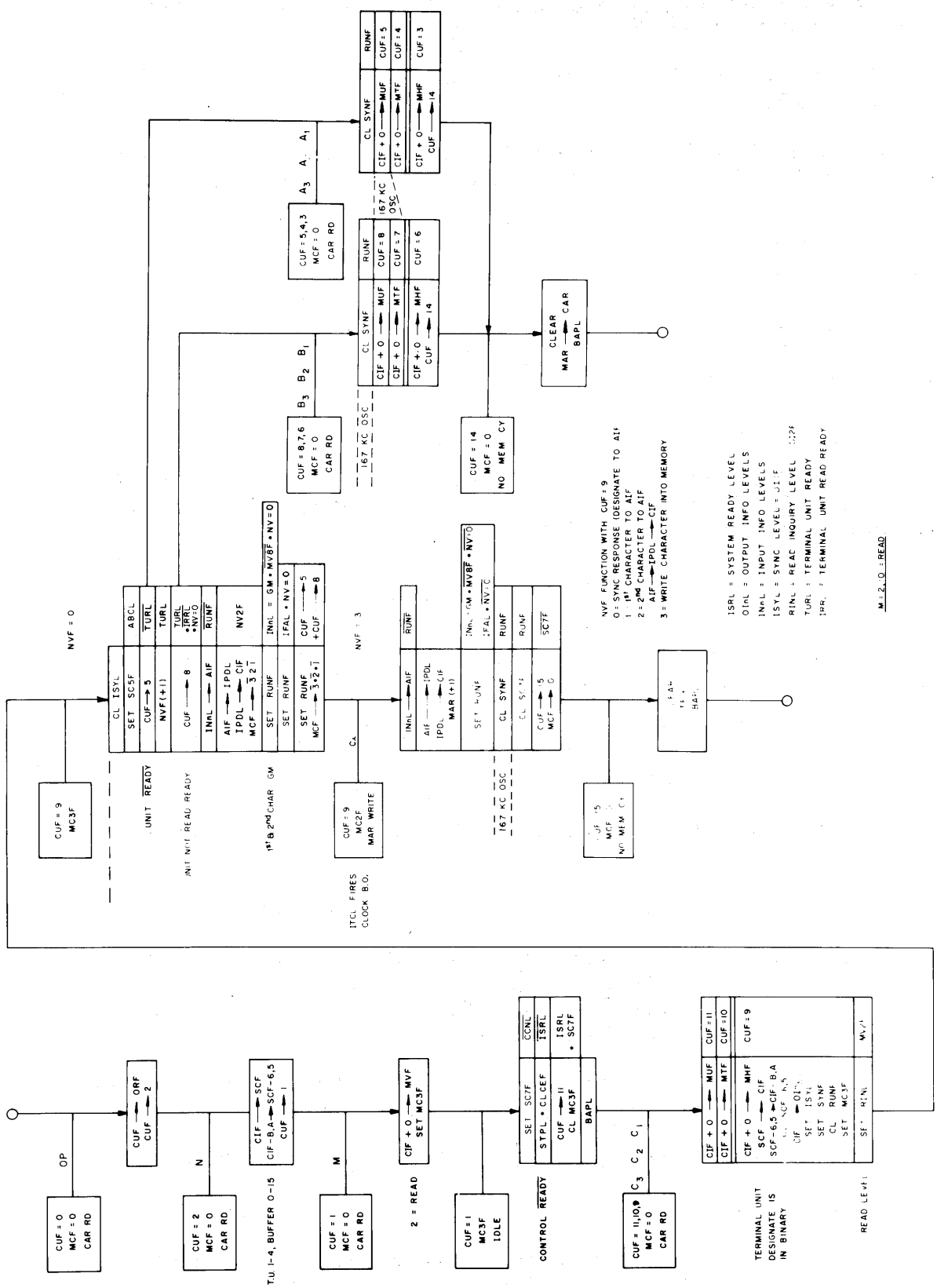


FIGURE II-23
B300 READ FLOW

Functional Detail

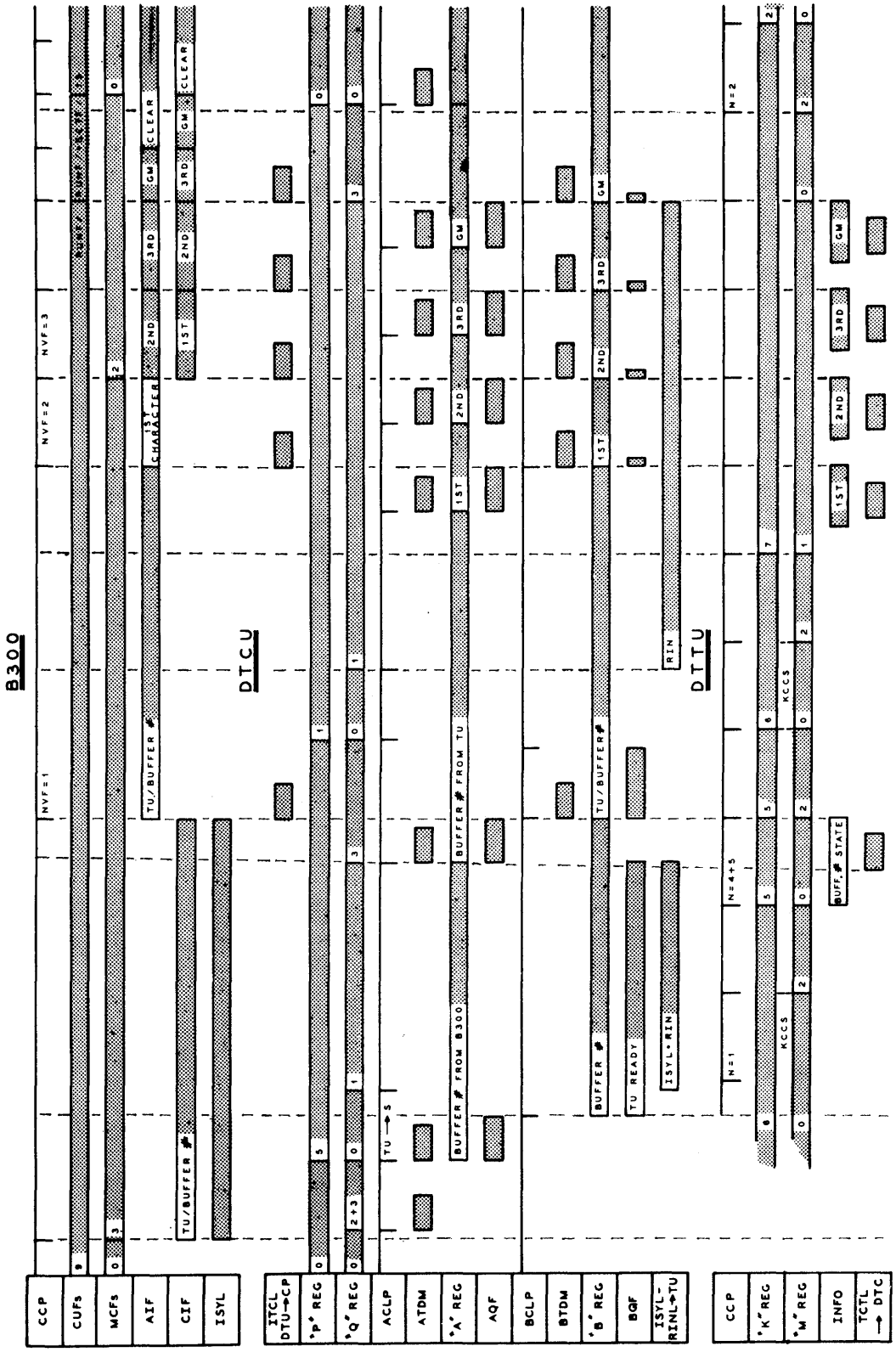


FIGURE II-24
B300 READ TIMING

CUF = 9 · MC3F

With its Clock under control of the DTCU, the Central Processor awaits a response from the DTCU and therefore the DTTU.

B249 DTCU

P = 0 · Q = 0 (A-Clock)

The A-Clock is enabled (ACL) by ISYL arriving from the B300. When the A-Clock pulse occurs, Q2F is SET. It is possible that Q1F could also be set if a Scan Cycle is in progress (SCA = 1).

P = 0 · Q = 2 + 3 (A-Clock)

The A-Clock remains enabled (ACL) by ISYL.

The Buffer number from the B300 is placed in the numeric portion of the "A" Register while the Zone positions are cleared. In conjunction with this, the "A" Register is marked "Occupied" by AQF being SET. The Zone bits of the DTTU/Buffer number character being sent from the B300 are placed into S1F and S2F while S4F and S8F are cleared. Note however, that the "S" Register is SET equal to 4 if the Zones are both OFF.

INAL · INBL/ - S = 1	INAL · INBL - S = 3
INAL/ · INBL - S = 2	INAL/ · INBL/ - S = 4

Since the Read operation is being called for, the B300 will send RIN (Read Inquiry) to the DTCU. This will cause "P" to be SET to 5 while "Q" is cleared.

If the B300 specifies Ignore-Group-Mark, MV8L will be true causing AAF to be SET. This will be transferred to IGMF (Ignore-Group-Mark Flip-flop) later on.

P = 5 · Q = 0 (B-Clock)

Refer to Figure II-10, Page 1 of 2.

Since P = 5 · Q = 0 was entered because of an A-Clock, ATDM will be ON for 4μs. When ATDM times out, a B-Clock pulse occurs. With the B-Clock, the Buffer number is transferred to the "B" Register, AQF is RESET and the Ignore-Group-Mark Flip-flop (IGMF) is SET if AAF is ON.

The Terminal is checked for POWER ON and REMOTE (TURL) and if it is Ready, BQF is SET. BQF remains OFF if the DTTU is Not-Ready. The DTTU must be checked for Ready at this time because P = 5 · Q = 1 depends on a Timing pulse from the DTTU. Therefore, Q = 1 must be bypassed when the DTTU is Not-Ready.

P = 5 · Q = 0 (A-Clock)

With AQF RESET, the A-Clock is enabled. When the Clock pulse occurs, the State of BQF which reflects the DTTU State is checked. With BQF ON, "Q" is SET to 1 to Sync with the DTTU. With BQF OFF, "Q" is SET to 3 to Sync with the System. R1F is SET to send the Not-Ready condition to System, and AQF is SET.

The Scan Flip-flop (SCAF) will be set if the Interrupt Flip-flop is ON and the selected DTTU does not have its Interrupt Flip-flop (N8F) ON as reflected by SIN = 0. This will allow the DTCU to scan for the DTTU that caused INTF to be ON after the Read Transfer is complete.

P = 5 · Q = 1 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

With P = 5; ISYL, the Buffer number held in the "B" Register, and RINL are SET to the DTTU.

The B249 now awaits a response from the Terminal Unit.

B487 - DTTU SYNC

N1F is SET by ISYS. Note that this is Floating logic and can occur on most "K" settings.

KCCS

Refer to Figure II-13.

When no Adapter requires attention (AANS), the following will take place:

1. SECS - The Buffer number is gated through the ECS (Entrance Character Switches) and placed in the "S" Register so that it can be used for addressing. This is accomplished by B3CS (B300 Connection) and RINL.

2. "K" is SET to 6 and "M" is SET to 2.

K = 6 · M = 2: SYSTEM ADDRESS ACCESS (SYNC)

Refer to Figure II-14.

The contents of the Add (Control) Cell are read and placed in the "DA" and "DB" Registers.

SRWS (System Read or Write) is true in that RINL is being SET from the DTCU. This, gated with PRWS (Permit Read or Write) says:

1. The Buffer is not is use by Adapter and is neither Write-Ready

nor Read-Ready. It is permissable to Read or Write and Idle Buffer.

or

2. The Buffer is Read-Ready (DA3F) and the operation at the Central Processor is not a Write.

or

3. The Buffer is Write-Ready and the operation at the Central Processor is not a Read.

N2F which signifies System Write, will remain OFF since RINL/ (Read Inquiry-Not) is required to SET it. The setting of N1F will determine whether or not the Group Mark is to be ignored. If IGMF is OFF in the DTCU denoting Read-To-Group-Mark, then N1F is RESET. If IGMF is ON denoting Ignore-Group-Mark, the N1F is not RESET.

Upon leaving KS06S (K = 6 · M = 2), the NU (N1F, 2, 4) should equal 4 signifying Read-To-Group-Mark or, N = 5, Ignore-Group-Mark.

K = 5 · M = 0 (KS05S)

Refer to Figure II-15.

The Buffer number as contained in the "S" Register is sent to the DTCU but is of no significance. The Read-Ready Level (IRRL) is sent to the DTCU signifying that the DTTU is in Sync. IRRL (Inquiry Read-Ready Level) can be generated in two ways:

1. By DA3F if the Buffer was Read-Ready.

2. By N = 4 + 5 if the Buffer was Idle.

ITCS (Inquiry Time for Character Switch) is generated 4μs. after Clock time and is sent to the DTCU where it becomes TCTS.

The DTCU will staticize the Buffer status and the Buffer type approximately 1μs. after TCTS arrives. At this time the DTCU sends ISYL/ to the Terminal.

Since ISYL/ arrives at the Terminal approximately 5μs. after the last Clock pulse, the DTTU Clock will continue to run.

The Sync between the DTCU and the DTTU is now complete. The DTTU will return to KCCS.

N4F ON (System Read or Write), causes "X", "Y" and "Z" to be transferred to the "D" Register. However, N4F will cause DA6F and DB6F to be SET, marking the Buffer In-Use-By-System. The Buffer number is transferred from the "S" to the "T" Register for temporary storage. This is necessary because some other Adapter may require attention and therefore, use of the "S" Register. The Interrupt Flip-flop (N8F) is RESET and the DTTU proceeds to K = 5 · M = 2 to store the Buffer status in Add.

K = 5 · M = 2 produces KCCS which allows checking for Attention Needed

from any Adapter including the one presently involved in the System Read.

The DTTU now waits for the Sync between the B300 and the B249 (DTCU) to be completed at which time the B249 will inform the DTTU that Information Transfer may take place by sending RINL (Read Inquiry).

B249

P = 5 · Q = 1 (A-Clock)

The DTCU has been idling at this point awaiting the DTTU response. The response will be the status of the addressed Buffer/Adapter along with the 4μs. Timing pulse TCTS. The Buffer number will also be sent but has no significance.

When TCTS arrives, an A-Clock will occur and the following action take place:

1. "R","T" ← DTTU State - The State of the addressed Buffer is staticized in the "R" Register where :
   a. R4F = Buffer Write-Ready.
   b. R3F = Buffer Read-Ready.
   c. R2F = Buffer Busy.
   d. R1F = Buffer Not-Ready.

   The Adapter type is staticized in the "T" Register to enable the proper translation:

   (1) T = 0 - Translate Baudot to BCL.
   (2) T = 1 - Translate ASCII to BCL.
   (3) T = 2 - No Translation.

2. A ← IN - Place the Buffer number into the numeric portion of the "A" Register. This will be passed along to the B300 but is of no significance.

3. AQF ← 1 - Mark the "A" Register "Occupied".
   BQF ← 0 - Mark the "B" Register "Occupied".

4. Q2F ← 1 - SET "Q" to 3.

P = 5 · Q = 3

During Q = 3, the DTTU/Buffer number and the Buffer status will be sent to the B300. Two B-Clocks will be produced to send this information to the Central Processor. The Central Processor will return ISYL = 0 to produce one A-Clock which provides Exit logic from Q = 3.

P = 5 · Q = 3 (B-Clock)

The first BCLP occurs when ATDM times out with the logic AQ = 1 · ATD = 0 · ISY = 1. With this pulse, the Buffer number is placed in the numeric portion of the "B" Register while the DTTU number is placed in BAF and BBF.

AQF is RESET and BQF is SET to mark the "B" Register "Occupied". BTDM is triggered and will send ITCL to the B300 when AQF changes State. AQF = 0 is included in this logic to provide a .5μs. delay to allow the "B" Register and Information Lines time to settle down.

The second BCLP simply clears BQF. The DTCU is now at P = 5 · Q = 3. An A-Clock with AQF and BQF RESET is awaiting ISY = 0 to be returned from the B300.

B300 OPERATION

CUF = 9 · MC3F

Refer to Figure II-23.

ITCL arriving at the Central Processor fires the Clock B.O. providing one CCP. The status of the DTTU is now checked for Unit-Ready and Read-Ready. If the DTTU is Not-Ready (non-existant Adapter or Data Set Not-Ready), TURL/ sent from the DTCU will SET CUF to 5 and SET RUNF. The AAA Branch is now taken.

If the DTTU is Ready(TURL) but Not Read Ready (IRRL/), CUF will be SET to 8 and RUNF will be SET resulting in the BBB Branch.

When the DTTU is Unit-Ready and Read-Ready, the NVFs will be counted from 0 to 1. The DTTU/Buffer number sent from the DTCU on the INnL lines is gated to the AIF but is of no significance. DI1F is RESET sending ISYL/ to take DTCU. The Central Processor is now at CUF = 9 MC3F · NVF = 1 · RUNF/. It is now waiting for the first Information character to be sent from the DTCU.

B249 OPERATION

P = 5 · Q = 3 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

When ISY = 0 arrives from the B300, the A-Clock pulse will be generated. With the A-Clock pulse, R3F is checked. If R3F is found OFF, the DTTU was not Read-Ready. Therefore, the operation is complete and the DTCU returns to P = 0 · Q = 0. If R3F is found ON, the DTTU is Read-Ready and the Information Transfer will take place. In this case, "P" is SET to 1 while "Q" is cleared.

P = 1 · Q = 0 (A-Clock)

Refer to Figure II-11.

The A-Clock is produced by the logic AQ = 0 · BQ = 0 · RR = 1; where as RR = 1 is produced by the DTTU "N" Register and is not dependent on the "K" Register setting in that Unit.

The A-Clock SETS Q = 1.

P = 1 · Q = 1 (A-Clock)

The DTCU A-Clock is now under control of the DTTU (TCTS). RINL is sent to the DTTU and the DTCU waits for information to arrive from the DTTU.

DTTU OPERATION

KCCS

Refer to Figure II-13.

When there is no Adpater requiring attention (AANS/), N4F along with RINS from the DTCU will transfer the Buffer number from the "T" to the "S" Register and will SET K = 6 · M = 2.

K = 6 · M = 2 · N4F (KT06S)

Refer to Figure II-16.

The ADD Cell is read, resulting in the "DA" and "DB" Registers being cleared with the exception of DA6F and DB6F. Since Memory Address portion of ADD was found cleared, DM00G (D Mostly Zero Gate) will be generated and will initialize the "X", "Y" and "Z" Registers. Initialization is accomplished by XYNS which transfers the Buffer number from the "S" Register to the "Y" Register, SETS X2F, and leaves X1F RESET. The "X","Y" and "Z" Registers now point at the first Information position of the Buffer.

The DTTU now proceeds to the System Read by setting K = 7 · M = 1.

K = 7 · M = 1 · N = 4 5

Refer to Figure II-17.

With each Clock pulse, the DTTU will perform a Buffer Read Cycle with Addressing under control of the "X" and "Y" Registers. The character held in "DA" or "DB" is placed on the Information Lines (INnL) to the DTCU via the "DC" lines under control of Z1F.

When Z1F is OFF, the character held in "DA" is sent to the DTCU (DCDAS). When Z1F is ON, the character held in "DB" is sent to the DTCU (DCDBS). Each Clock pulse will increment the Address in the "X","Y" and "Z" Registers in the following manner:

1. ZCS - Always complements Z1F.
2. ZCS · Z1F - Increments "X" by one (XYCS).
3. X = 15 · XYCS - Increments "Y" by one.

When "X" is found equal to 15, it is incremented to 2. This bypasses the ADD and I/O portions of the next Memory Plane.

The action of reading a cell and incrementing the Address continues until one of three things occur:

1. A Group Mark occurs and the instruction specified Read-To-Group-Mark (NIF/).
2. The entire Buffer has been transferred (BFLS).
3. Some Adapter requires attention (AANS) causing an Interrupt of the System Read.

CHARACTER TIMING - DTTU TO DTCU

Refer to Figure II-24.

Each Clock pulse in the DTTU fires a 4μs. Multi (ITCM-1). When an ITCM-1 times out, it fires a second 4μs. Multi (ITCM-2). The 4μs. output of ITCM-2 is sent to the DTCU as TCTL (Terminal Character Time Level). TCTL produces one A-Clock pulse in the DTCU.

Each Clock pulse in the DTTU initiates a Buffer Read Cycle such that the information read from Core is strobed into the "D" Register 3μs. after the Clock pulse. The character is gated to the INnLs as soon as it reaches the "D" Register.

TCTL will reach the DTCU 4μs. after DTTU Clock Time. When the A-Clock pulse occurs in the DTCU, the character is transferred to the "A" Register.

DTCU OPERATION

P = 1 · Q = 1 (A-Clock)

Refer to Figure II-11.

When a character is on the Information Lines from the DTTU, it will be accompanied by the 4μs. pulse TCTS. TCTS produces an A-Clock which will place the character into the "A" Register and will SET AQF marking the "A" Register "Occupied".

P = 1 (Universal State)

Once the character is in the "A" Register, it is submitted to the Translator where the encoded output is selected by the "T" Register.

P = 1 · BQF = 0 (B-Clock)

4μs. after the character was placed in the "A" Register, ATDM will time out, enabling the B-Clock. With a B-Clock, the character is transferred from the Encoder outputs of the Translator into the "B" Register, BQF is SET, AQF is RESET, and BTDM is triggered.

P = 1 (Universal State)

As soon as the character reaches the "B" Register, it is on the Information Lines to the B300. ITCL (Inquiry Time for Character Level) is sent to the B300 with BTDM and AQ = 0. AQ = 0 is again gated with the logic for ITCL to provide a slight delay.

B300 OPERATION

CUF = 9 · MC3F

Refer to Figure II-23.

The NVF was stepped to 1 during the Sync. This occurred when the DTCU sent the Buffer number and ITCL. This Buffer number is in the AIF, but is of no significance.

After the DTCU has the first character to be stored on the INnLs, it provides ITCL for the Central Processor. ITCL fires the Clock B.O., providing a CCP.

The NVFs are now stepped to 2, and the first character is placed in the AIFs. When the second character is available from the DTCU, ITCL once again provides a CCP for the Central Processor. Because NV2F is now found ON, the first character being held in the AIFs is transferred to the CIFs and the MCFs are SET to 2. This initiates a MAR Write to store the first character while the second character is transferred from the INnLs to the AIFs.

CUF = 9 · MC2F

Each ITCL will provide a CCP which will do the following:

1. Transfer a character from AIF to CIF.
2. Count MAR + 1.
3. Initiate a MAR Write to store that character.
4. Place a new character in the AIF.

This process will continue until the complete message has been transferred to the Central Processor.

There are two ways in which the System Read can be terminated:

1. Arrival of a Group Mark on the INnLs when the Read instruction

specified Read-To-Group-Mark (MV8L/).

2. Encountering the Final Address in the DTTU (IFAL).

When either of these situations occurs, the Final Character to be stored will be placed in the AIF, and RUNF will be turned ON. The Central Processor is back on its own Clock. The next CCP will transfer the Final Character to the CIFs and will initiate a MAR Write to store that character. This CCP finding RUNF ON, will clear SYNF and SC7F. The next CCP will occur after the Final Character has been stored and will find SC7F/. This will provide the logic to SET CUF = 15 · MCF = 0 to Exit the instruction.

OVERALL

Refer to Figure II-24.

Each CCP in the DTTU causes a character to be read from the Buffer and 4μs. later, it sends the 4μs. Timing pulse (TCTL), to the DTCU. TCTL, arriving at the DTCU, generates an A-Clock which places the character into the "A" Register and triggers ATDM. When ATDM times out 4μs. later, a B-Clock transfers the character (after translation) into the "B" Register and triggers BTDM to provide ITCL to the B300.

Once a character is in the "B" Register, it is available to the B300. ITCL at the B300 produces a CCP which:

1. Initiates a Memory Cycle to store the last character to arrive from the DTCU.

2. Place the new character into AIF.

DTTU SYSTEM READ TERMINATION

The System Read can be terminated in two ways:

1. Recognition of a Group Mark when the System specified Read-To-Group-Mark (N1F/).

2. Buffer-Final-Location has been reached (BFL).

K = 7 · M = 1

Refer to Figure II-17.

When a Group Mark has been read from the Buffer into the "DA" or "DB" Register, it will generate EISS (End of Information Segment). EISS, gated with N1F/ which denotes Read-To-Group-Mark, will clear M1F and SET L2F.

When the last character in the Buffer has been read and sent to the Central Processor, BFLS (Buffer-Final-Location) gated with Z1F will clear M1F and SET L2F.

K = 7 · M = 0

L2F generates CWT to be sent to all Adapters. In the designated Adapter, CWT gates the status of the Adapter back on the AC lines as well as RESETTING the Adapter-Special-Condition Flip-flops. The Adapter status is transferred from the ACn (Adapter Character) to the EC (Entrance Character) lines with ECACS, and thence to the "DA" Register and DB1F.

The "N" Register is SET to 2 to initiate a Buffer Scan Cycle.

K = 7 · M = 2 (ADD WRITE)

The Adapter status is stored in ADD. The DTTU is now at KCCS, and the System Read is complete.

DTCU

As each character arrives from the DTTU, it will be accompanied by TCT (Terminal Time for Character). TCT will produce an A-Clock pulse which will place the character in the "A" Register.

When the A-Clock occurs, ATDM is triggered. 4μs. later, a B-Clock transfers the character to the "B" Register and therefore makes it available to the B300. This action continues until:

1. A Group Mark has been sent from DTTU and the B300 instruction specifies Read-To-Group-Mark (MV8).

2. The character arriving from DTTU came from its Final-Buffer-Location (BFL).

DTCU GROUP MARK ENDING

When a Group Mark arrives from the DTTU, it is placed into the "A" Register. The subsequent B-Clock which transfers the Group Mark to the "B" Register will find EGM = 1 · IGM = 0 where:

1. EGM = 1 says a Group Mark is on the Encoder output of the Translator.

2. IGM = 0 says the Ignore-Group-Mark Flip-flop is OFF, denoting the B300 MV8F is OFF.

The result of this logic is to SET Q = 3 while transferring the Group Mark to the B300.

P = 1 · Q = 3 (A-Clock)

Refer to Figure II-11.

This is Exit logic.

When the DTTU has changed its State as signified by RR = 0 (DTTU Not-Read-Ready), and at least 4μs. has elapsed since the last B-Clock (BTDM/), an A-Clock will occur.

This A-Clock will clear the "P" and "Q" Registers ending the System Read.

B300 DATA COMMUNICATION WRITE

Reference Figures II-25 and II-27.

The Write instruction will transfer the contents of a specified area of B300 Core to the DTCU (B249) where the information is translated and then sent to a specific Buffer in the DTTU (B487).

The Write is initiated by the B300. The Central Processor sends a six bit character to the DTCU defining the Terminal Unit and Buffer it wishes to Write to. Along with this character, the B300 sends several Control Levels, the most important of which are ISYL (Sync) and WINL (Write).

The DTCU places the Zone bits of that character in its "S" Register so that it points to the specified DTTU. The numeric bits (Buffer number) are placed in the DTCU "A" Register, transferred to the "B" Register, and then sent to the selected DTTU. The Sync Level (ISYL) and the Write Level (WINL) will accompany the Buffer number sent to the DTTU.

The DTTU, recognizing the Sync and Write Control Levels, will place the number of the Buffer to be written into its "S" Register and will then proceed through the Sync Cycle.

As a result of the DTTU Sync, the status of the Buffer to be written and the type of Adapter are sent to the DTCU. At the DTCU, this information is staticized into the "R" and "T" Registers respectively. The DTTU is released back to the Idle State (KCCS) while the DTCU passes along to the B300 status of the Addressed Buffer.

The B300 samples the status lines to determine whether or not the Write can take place. If the Buffer cannot be written to, the DTCU will send IWRL/ (Inquiry Write-Ready-Not) causing the B300 to take the BBB Branch.

If the DTCU returns TURL/ (DTTU Not-Ready), the B300 will take the CCC Branch. If neither of these conditions exist, the Write Transfer will take place.

The Timing for the Write is controlled by the DTTU where information is transferred at its Clock rate (10μs/character). After information becomes available from the DTCU, each Clock pulse in the DTTU will cause the character to be stored in the Buffer. As a character is being stored, the 4μs Timing pulse TCTL is sent to the DTCU.

Functional Detail

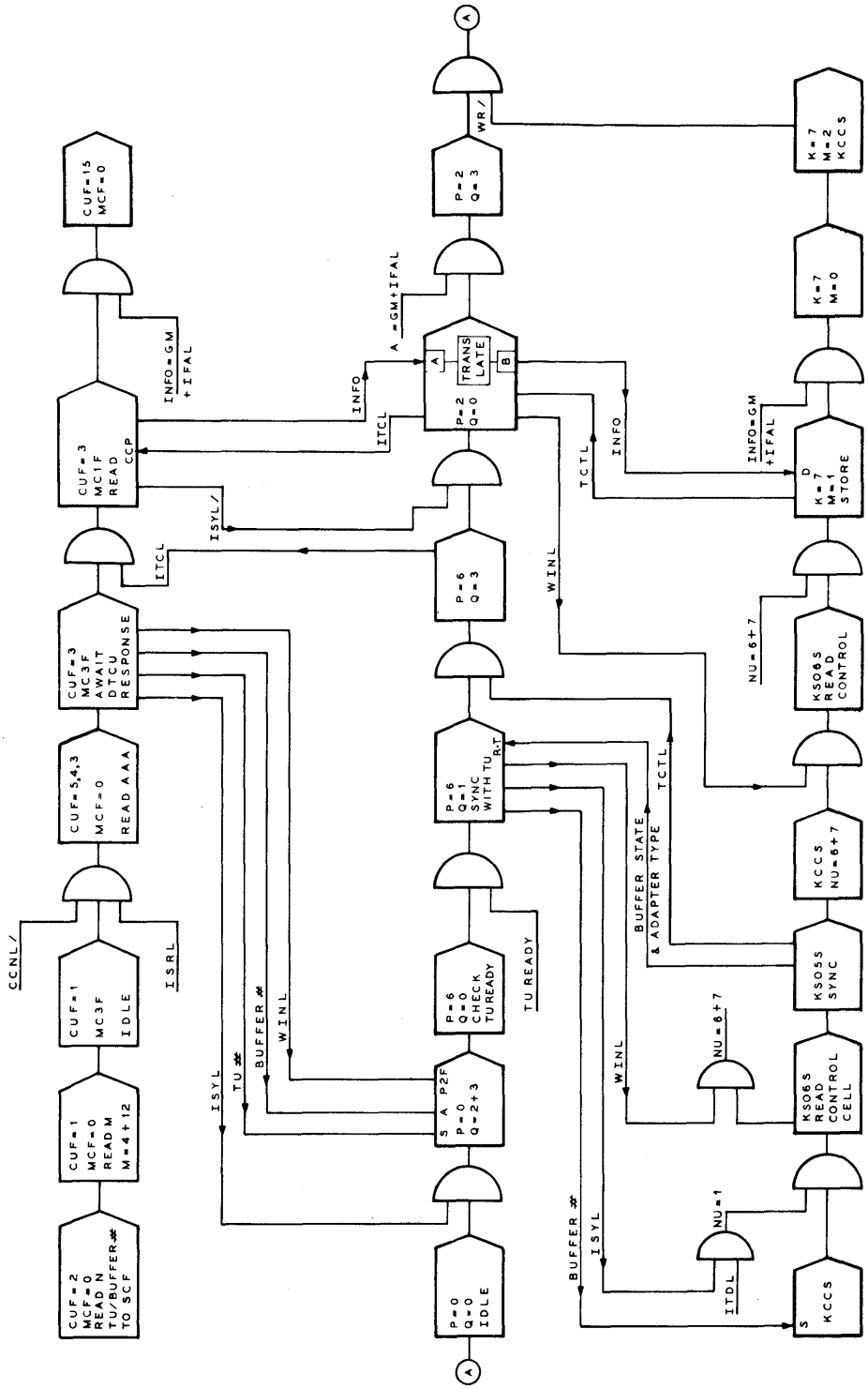


FIGURE II-25
B300 WRITE - BLOCK FLOW

TCTL at the DTCU, causes a character to be transferred from the "A" Register, through the Translator, and into the "B" Register. Once this character reaches the "B" Register, the "A" Register is free to accept another character from the B300.

Whenever a character reaches the "B" Register, a Timing pulse (ITCL) is sent to the B300 informing it that a new character may be placed on the Information Lines to the DTCU.

The B300, recognizing ITCL, will produce a CCP initiating a Memory Cycle to read the next character. This process continues until a Group Mark is recognized or, the Final Location of the Buffer being written to has been reached. In either case, the three Units will be released in the following order:

1. B300.
2. DTTU.
3. DTCU.

DETAILED DESCRIPTION

OP = L = 35
M = 4 Write-To-Group-Mark.
M = 12 Ignore Group Mark.
N = Numeric - Buffer number 0 through 15.
Zone - DTTU number.
AAA = Information Field.
BBB = Branch if Buffer is Read-Ready.
CCC = DTTU Not-Ready Branch.

When M = 4, the Write will be terminated when encountering a Group Mark. When M = 12, Group Mark will be ignored and the Write will be terminated when the Final Location in the DTTU Buffer has been filled.

It is permissable to Write to an Idle or Write-Ready Buffer, but NOT to a Read-Ready or Busy Buffer.

B300 OPERATION

CUF = 2 · MCF = 0

Refer to Figure II-26.

The Buffer is placed in the SCF 1 through 4, while the DTTU number is placed in the SCF 5 and 6.

Functional Detail

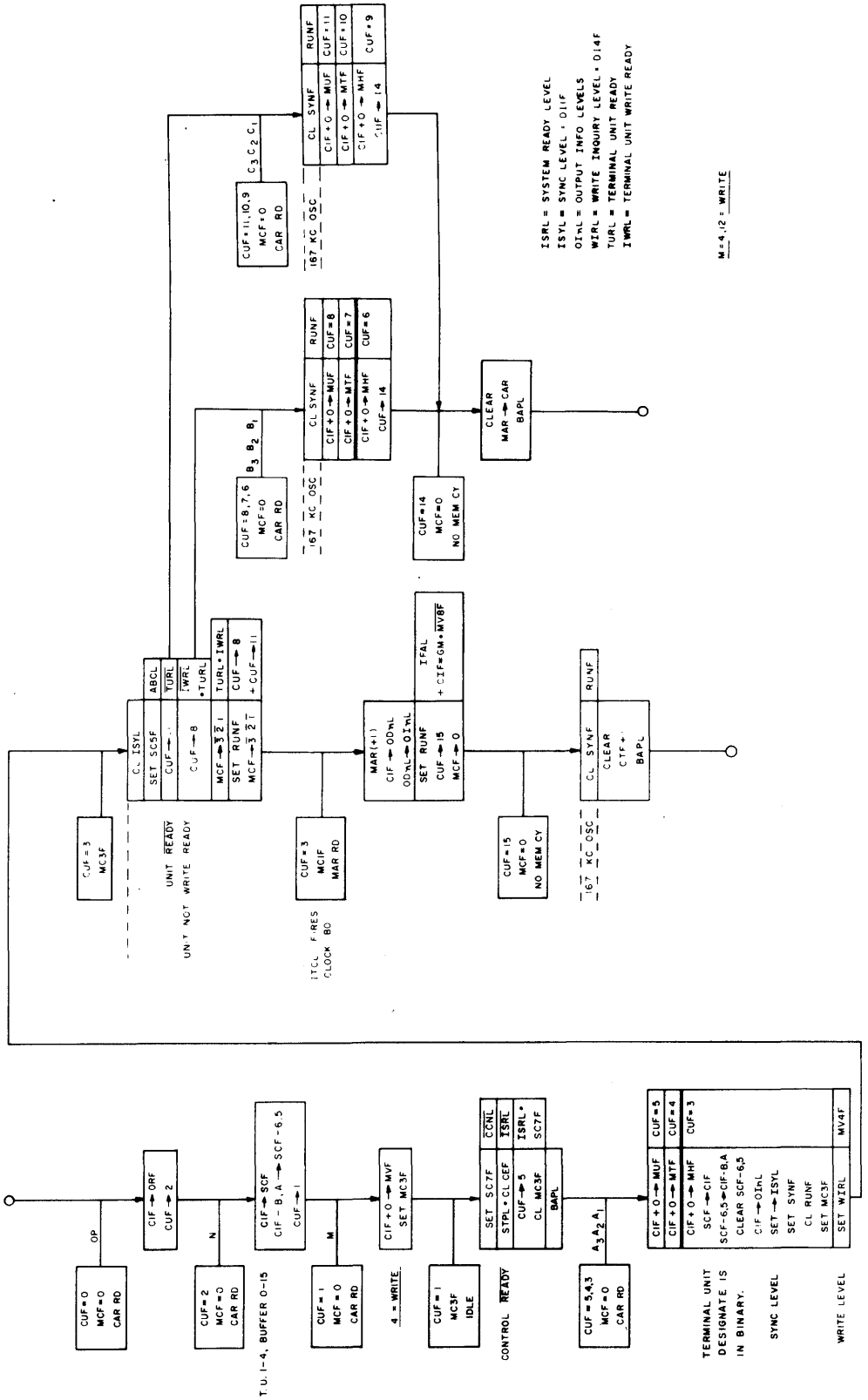


FIGURE II-26
B300 WRITE FLOW

Functional Detail

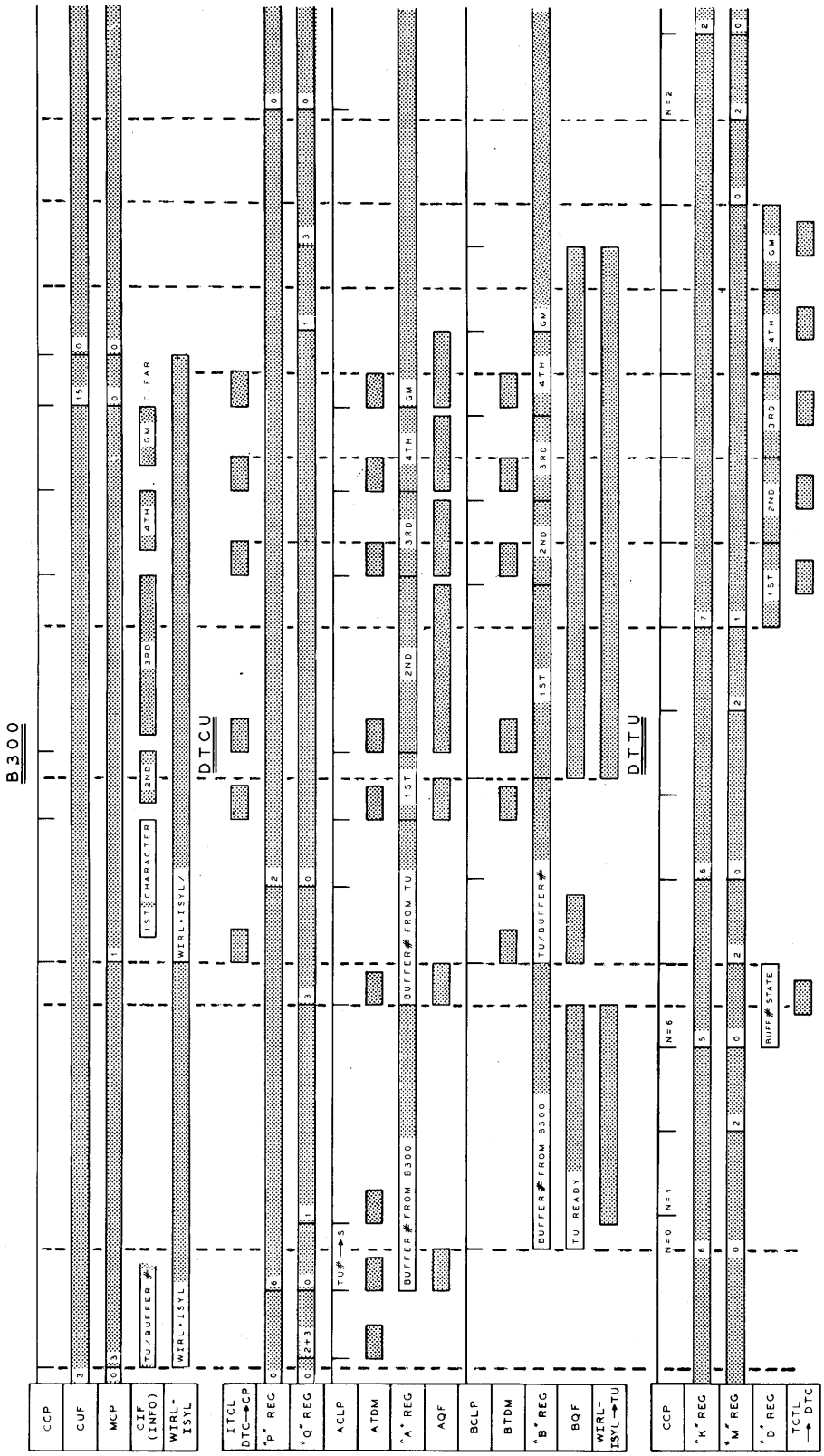


FIGURE II-27
B300 WRITE TIMING

CUF = 1 · MCF = 0

The "M" Variant is read and placed in the MVFs. The 4-bit must be ON for a Write instruction. The 8-bit ON, denotes Ignore-Group-Mark.

CUF = 5, 4, 3 · MCF = 0

While the final digit of the AAA Address is being placed in MAR, the following actions take place:

1. SCF → CIF - Place the DTTU Buffer number in CIF.
   CIF → OInL - Output Information Lines. Note that the transfer of CIF to OInL is binary. This is necessary because Internal Zero would translate to a BCL 10 which would confuse the DTCU.
2. SET ISYL - The actual logic here is SET to DI1F which sends ISYL (Inquiry Sync Level) to the DTTU.
3. SET WIRL - DI4F is SET and sends WIRL (Write Inquiry Level) to the DTCU.
4. SET SYNF - Clear RUNF turning Central Processor Clock Control over to the DTCU.

At this point, the B300 waits for the DTCU and the DTTU to SYNC.

DTCU (B249)

P = 0 · Q = 0 (A-Clock)

Refer to Figure II-9.

The A-Clock is enabled (ACL) by ISYL arriving from the B300. When the A-Clock pulse occurs, Q2F is SET. It is possible that Q1F could also be set if a Scan Cycle is in progress (SCA = 1).

P = 0 · Q = 2 + 3 (A-Clock)

The A-Clock remains enabled (ACL) by ISYL.

The Buffer number from the B300 is placed in the numeric portion of the "A" Register while the Zone positions are cleared. In conjunction with this, the "A" Register is marked "Occupied" by AQF being SET. The Zone bits of the DTTU/Buffer number character being sent from the B300 are placed into S1F and S2F while S4F and S8F are cleared. Note, however, that the "S" Register is SET equal to 4 if the Zones are both OFF.

INAL · INBL/ - S = 1	INAL · INBL - S = 3
INAL/ · INBL - S = 2	INAL/ · INBL/ - S = 4

Since a Write operation is being called for, the B300 will send WINL (Write Inquiry Level) to the DTCU. This will cause the "P" Register to be SET to 6, while "Q" is cleared.

If the B300 specifies Ignore-Group-Mark, MV8L will be true causing AAF to be SET. This will be transferred to IGMF (Ignore-Group-Mark) later on.

P = 6 · Q = 0 (B-Clock)

Refer to Figure II-10, Page 1 of 2.

Since P = 6 · Q = 0 was entered because of an A-Clock, ATDM will be ON for 4μs. When ATDM times out, a B-Clock pulse occurs. With the B-Clock, the Buffer number is transferred to the "B" Register, AQF is RESET, and the Ignore-Group-Mark Flip-flop (IGMF) is SET if AAF is ON. The Terminal is checked for POWER ON and REMOTE (TURL) and if it is Ready, BQF is SET.

BQF remains OFF if the DTTU is Not-Ready. The DTTU must be checked for Ready at this time because P = 6 · Q = 1 depends on a Timing pulse from the DTTU. Therefore, Q = 1 must be bypassed when the DTTU is Not-Ready.

P = 6 · Q = 0 (A-Clock)

With AQF RESET, the A-Clock is enabled. When the Clock pulse occurs, the state of the BQF which reflects the DTTU State is checked. With BQF ON, the "Q" Register is SET to 1 to Sync with the DTTU. With BQF OFF; "Q" is SET to 3 to Sync with the System, R1F is SET to send the Not-Ready condition to System, and AQF is SET.

The Scan Flip-flop (SCAF) will be set if the Interrupt Flip-flop is ON and the selected Data Transmission Terminal Unit does not have its Interrupt Flip-flop (N8F) ON as reflected by SIN = 0. This will allow the DTCU to scan for the DTTU that caused INTF to be ON. The scan will take place after the Write Transfer is complete.

P = 6 · Q = 1 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

With P = 6; ISYL, RINL, and the Buffer number held in the "B" Register are sent to the DTTU.

The B249 now awaits a response from the Terminal Unit.

DTTU OPERATION

ISYS arriving at the DTCU sets NU = 1, provided there is no Scan Cycle taking place (NU = 0) and the DTTU is designated (ITDL).

KCCS

Refer to Figure II-13.

The Buffer number that the System (B300) wishes to write into is on the ECn (Entrance Character) lines (ECSYS). When no Adapter requires attention, this number is placed in the "S" Register with SECS and the DTTU proceeds to a System Sync. The logic to transfer EC to the "S" Register is as follows:

SECS = AANS/ · NU = 1 · B3CS · (RINS + WINS)

Where:

AANS/ - No Adapter requires attention.

NU = 1 - The Central Processor has initiated some activity (ISYL).

B3CS - Connection is to the B300.

RINS + WINS - The System activity is a Read or Write as opposed to an Interrogate.

K = 6 · M = 2: SYSTEM ADDRESS ACCESS (SYNC)

Refer to Figure II-14.

The contents of the ADD (Control) Cell are read and placed in the "DA" and "DB" Registers. SRWS (System Read or Write) is true in that WINL is being sent from the DTCU. This, gated with PRWS (Permit Read or Write), will SET N4F signifying a System Read or Write. Aside from Test conditions, PRWS (Permit Read or Write) denotes one of the following:

1. The Buffer is Not-In-Use by the Adapter and is neither Write-Ready nor Read-Ready. It is permissable to Read or Write an Idle Buffer.

2. The Buffer is Read-Ready (DA3F) and the operation at the Central Processor is not a Write.

3. The Buffer is Write-Ready and the operation at the Central Processor is not a Read.

N2F, which signifies System Write, will be SET by RINL/ (Read Inquiry-Not). The status of N1F will determine within the DTTU, whether or not the Group Mark is to be ignored. If MV8F is OFF in the Central Processor denoting Read-To-Group-Mark, then N1F is RESET.

If MV8F is ON denoting Ignore-Group-Mark, then N1F remains SET. Upon leaving KS06S (K = 6 · M = 2), the "NU" Register should equal 6 or 7. NU = 6 signifies Write-To-Group-Mark. NU = 7 means Ignore-Group-Mark.

K = 5 · M = 0 (KS05S)

Refer to Figure II-15.

The Buffer number contained in the "S" Register is sent to the DTCU but is of no significance. The Write-Ready Level (IWRL) is sent to the DTCU to inform it that the DTTU is in Sync. IWRL can be generated in two ways:

1. By DA4F if the Buffer was Write-Ready.
2. By NU = 6 + 7 if the Buffer was Idle.

The 4μs. pulse TCTS (Terminal Character Time), is sent to the DTCU to provide it with a Clock pulse.

The DTCU will staticize the Buffer status and the Buffer type approximately 1μs. after TCTS arrives. At this time, the DTCU sends ISYL/ to the Terminal.

Since ISYL/ arrives at the Terminal approximately 5μs. after the last Clock pulse, the DTTU Clock will continue to run.

The Sync between the DTCU and the DTTU is now complete. The DTTU will return to KCCS.

B249

P = 6 · Q = 1 (A-Clock)

The DTCU has been idling at this point awaiting the DTTU response. The response will be the status of the addressed Buffer/Adapter along with the 4μs. Timing pulse TCTS. The Buffer number will also be sent but has no real significance.

When TCTS arrives, an A-Clock will occur at which time the following actions take place:

1. R, T ← DTTU STATE - The State of the addressed Buffer is staticized in the "R" Register where:
   a. R4F = Buffer Write-Ready.
   b. R3F = Buffer Read-Ready.
   c. R2F = Buffer Busy.
   d. R1F = Buffer Not-Ready.

   The Adapter type is staticized in the "T" Register to enable the proper translation:

   a. T = 0 - Translate BCL to Baudot.
   b. T = 1 - Translate BCL to ASCII.
   c. T = 2 - No Translation.

2. A ← IN - Place the Buffer number into the numeric portion of the "A" Register. This will be passed along to the B300, but is of no significance.

3. AQF ← 1 - Mark the "A" Register "Occupied".
   BQF ← 0 - Mark the "B" Register "Occupied".

4. Q2F ← 1 - SET "Q" to 3.

P = 6 · Q = 3

During Q = 3, the DTTU/Buffer number and the Buffer status will be sent to the B300. Two B-Clocks will be produced to send this information to the Central Processor. The Processor will return ISYL = 0 to produce one A-Clock which provides Exit logic from Q = 3.

P = 6 · Q = 3 (B-Clock)

The first BCLP occurs when ATDM times out with the logic AQ = 1 · ATD = 0 · ISY = 1. With this pulse, the Buffer number is placed in the numeric portion of the "B" Register while the DTTU number is placed in BAF and BBF. AQF is RESET and BQF is SET to mark the "B" Register "Occupied". BTDM is triggered and will send ITCL to the B300 when AQF changes State. AQF = 0 is included in this logic to provide a .5μs. delay to allow the "B" Register and Information Lines time to settle down.

The second BCLP simply clears BQF. The DTCU is now at P = 6 · Q = 3. An A-Clock with AQF and BQF RESET is waiting for ISY = 0 to be returned from the B300.

B300 OPERATION

CUF = 3 · MC3F

Refer to Figure II-26.

ITCL arriving at the Central Processor fires the Clock B.O. providing one CCP. The status of the DTTU is now checked for Unit-Ready and Write-Ready. If the DTTU is Not-Ready, TURL/ will SET CUF to 11 and SET RUNF. The CCC Branch will now be taken. If the DTTU is Ready (TURL) but not Write-Ready (IWRL/), CUF will be SET to 8 along with RUNF, resulting in the BBB Branch.

When the DTTU is Ready and Write-Ready, the MCFs will be SET to 1 and the first Memory Read Cycle will be initiated making the first character to be stored in the DTTU Buffer available on the OInLs (Output Information Lines) to the DTCU. Along with this first character, DI1F will will be cleared providing ISYL/ to the DTCU.

B249 OPERATION

P = 6 · Q = 3 (A-Clock)

Refer to Figure II-10, Page 2 of 2.

When ISY = 0 arrives from the B300, an A-Clock pulse will be generated. R4F is checked with the A-Clock. If R4F is found OFF, the DTTU was not Write-Ready. Therefore, the operation is complete and the DTTU returns to P = 0 · Q = 0. If R4F is found ON, the DTTU is Write-Ready and the Information Transfer will take place.

In this case, the "P" Register is set to 2 while "Q" is cleared.

P = 2 · Q = 0 (A-Clock)

Refer to Figure II-12, Page 1 of 2.

The A-Clock is enabled by AQ = 0 · WIN = 1. When the A-Clock pulse occurs, the first information character from the B300 is loaded into the "A" Register (A ← IN) and AQF is SET, marking the "A" Register as "Occupied". This A-Clock also triggers ATDM and BTDM.

P = 2 (Universal State)

The character in the "A" Register is sent through the Translator where the correct translated bit configuration is placed on the Encoder lines according to the "T" Register.

With BTDM and ATDM both triggered, the 4μs Timing pulse ITCL (Inquiry Time for Character Level) is sent to the B300 requesting the next character.

P = 2 · DTT = 1 · BQ = 0 · DQ = 0 · B-Clock

A B-Clock is produced by AQ = 1 · ATD = 0 · WR = 1 where:

1. AQ = 1 · ATD = 0 says there is a character in the "A" Register and the character has been available to the Translator for 4μs.

2. WR = 1, the DTTU is Write-Ready as indicated by the "N" Register. This term is not dependent on any "K" Register setting in the DTTU. The translated character is transferred from the Encoder to the "B" Register (B ← E) with a B-Clock pulse. BQF is SET marking the "B" Register "Occupied" and AQF is RESET, marking the "A" Register "Occupied.

At this point, there are two blocks of logic in effect. These are:

P = 2 · AQ = 0 · A-Clock and P = 2 · DTT = 1 · BQ = 1 · DQ = 0 · B-Clock.

P = 2 · DTT = 1 · BQ = 1 · DQ = 0 · B-Clock.

Refer to Figure II-12, Page 2 of 2.

As soon as BQF is SET, it sends WINL to the DTTU. This is the only action that will take place under this Flag until the DTTU responds after it has accepted the first character. At this time, the DTTU will return TCTL (Terminal Character Time Level) requesting the next character.

P = 2 · AQ = 0 (A-Clock)

Refer to Figure II-12, Page 1 of 2.

When a character has been accepted by the "B" Register, AQF is RESET, enabling the A-Clock. When the A-Clock occurs, the next character will be placed in the "A" Register while AQF is SET, marking the "A" Register "Occupied". The ACLP will also trigger ATDM and BTDM.

P = 2 (Universal State)

ATDM and BTDM occurring in concert, send ITCL (Inquiry Time for Character Level) to the B300 requesting the next character.

DTTU OPERATION

KCCS

Refer to Figure II-13.

When there is no Adapter requiring attention (AANS/), N4F along with WINL will transfer the Buffer number from the "T" Register to the "S" Register and SET K = 6 · M = 2.

K = 6 · M = 2 · N4F (KT06S)

Refer to Figure II-16.

The ADD (Control) Cell is read resulting in the "DA" and "DB" Registers being cleared, with the exception of DA6F and DB6F. This will produce DM00G (D Mostly Zero Gate) which will initialize the "X","Y" and "Z" Registers. Initializiation is accomplished by XYNS which transfers the Buffer number from the "S" to the "Y" Register, SETS X2F and leaves Z1F RESET. The "X", "Y" and "Z" Registers now point at the first Information position of the Buffer.

Since the B300 and the DTCU have already processed the first character to be stored, this character is now available on the EC (Entrance Character) lines. This first character is placed in the "DA" Register (DAECS) while the "DB" Register is cleared (DBKS). This results because N2F is ON and DA1F, which represents the status of Z1F, is OFF. The DTTU now proceeds to the System Write by SETTING K = 7 · M = 1.

K = 7 · M = 1 · N = 6 + 7

Refer to Figure II-18.

The character being held in the "DA" Register is stored in the Buffer

while the "DB" portion of the Cell is allowed to re-circulate. This action is under control of Z1F. When Z1F is OFF, the Read Strobe for "DA" is inhibited (HRDAS), while the Read Strobe for "DB" is allowed.

TCTL is sent to the DTTU so that the next character to be stored will be available prior to the next DTTU Clock pulse. When the Clock pulse occurs, the Address in the "X", "Y" and "Z" Registers is incremented and the new character is placed into "DA" or "DB" according to the State of Z1F.

Considering the second character, Z1F will be found OFF, enabling the term DBECS which will transfer the character on the EC lines to the "DB". Since the Address is being incremented, Z1F will be SET so that during the Memory Cycle, HRDBS will inhibit the "DB" Read Strobe while the character in the "DA" portion of the Cell is allowed to re-circulate. During the Write portion of the Memory Cycle, ITCL is sent to The DTCU so that it will make available the next character to be placed in the DTTU Buffer.

OVERALL

The transfer is started when the DTCU sends ITCL to the B300. Upon receipt of ITCL, the B300 reads a character and places it on the Information Lines to the DTCU.

At the DTCU, an ACLP places the first character into the "A" Register. 4μs. later, a BCLP transfers the first character into the "B" Register. When character number one reaches the "B" Register, BQF is SET and sends WINL to the DTTU. The B487 (DTTU) receiving WINL, proceeds through Address Access to Information Transfer, and stores the first character. 4μs. after the character reaches the "DA" Register, TCTL is sent to the DTCU requesting the next character.

At the DTCU, the Timing pulse TCTL produces a B-Clock, transferring a character from the "A" Register through the Translator into the "B" Register. The B-Clock RESETS AQF, enabling the A-Clock to bring the next character into the "A" Register. The A-Clock triggers ATDM and BTDM which sends ITCL to the B300 which produces a CCP to read the next character from System Memory.

ENDINGS

Write Terminated At The Group Mark

Refer to Figure II-26.

The B300 reading the Group Mark, will hold it in the CIFs until the DTCU signals that it has accepted it. When an A-Clock places the Group Mark into the "A" Register, ITCL will be sent to the B300 (ATDM · BTDM). At the B300, the CCP produced by ITCL will SET RUNF, CUF to 15, and MCF to 0 completing the instruction provided MV8F is OFF denoting End-At-Group-Mark.

DTCU (B249)

Refer to Figure II-12, Page 2 of 2.

The BCLP which transfers the Group Mark to the "B" Register will, recognizing the Group Mark in the "A" Registerm SET Q = 1. While the DTTU is storing the Group Mark, TCTL will cause a B-Clock which, finding Q = 1; will SET Q = 3.

The DTCU will now wait at P = 2 · Q = 3 · A-Clock for the DTTU to change State by setting NU = 2.

DTTU

Refer to Figure II-18.

The DTTU recognizing that the Group Mark has been stored, will proceed to K = 7 · M = 0 and K = 7 · M = 2 and back to KCCS, completing the operation.

P = 2 · Q = 3 (A-Clock)

Refer to Figure II-12, Page 1 of 2.

After the DTTU changes its "N" Register setting to 2, WR = 0 (Write-Ready-Not) will enable the DTCU A-Clock. The ACLP will clear the "P" and "Q" Registers thus ending the operation.

WRITE TERMINATED AT BFL ENDING

As the DTTU accepts the character to be stored in the next to last position of the Buffer, BFL (Buffer-Final-Location) is sent to the DTCU. The DTCU recognizes BFL with the BCLP that places the Final Character to be transferred into the "B" Register, at which time the "Q" Register is SET to 2.

As the Final Character is placed in the "B" Register, an A-Clock is allowed. This places an extra character in the "A" Register and SETS Q = 3.

After the DTTU has stored the Final Character, it proceeds through K = 7 · M = 0, K = 7 · M = 2 and changes the "N" Register to 2. This sends WR = 0 (Write-Ready-Not) to the DTCU.

The DTCU at P = 2 · Q = 3, produces an A-Clock when WR = 0 arrives from the DTTU, clearing the "P" and "Q" Registers. This completes the operation.

When the "Q" Register is SET to 2, IFAL is sent to the B300 with the final ITCL. The B300, recognizing IFAL (Inquiry Final Address Level) with a CCP, SETS RUNF, CUF to 15, and MCF to 0 completing the instruction.

✓ B300 PASSIVE INTERROGATE - ITU (B486) MODE

GENERAL DESCRIPTION

OP = L = 35

M = 1

N = 0

AAA = Branch to when any CTU is Read-Ready.

BBB = Location of the CTU number that is Read-Ready.

CCC = Write-Ready Branch N/A with CTU.

When functioning with an On Line Teller System, the Passive Interrogate serves two purposes:

1. Inform the B300 of an Interrupt condition (B486 Read-Ready).

2. Inform all CTU's (B486) that the Data Processor is active.

The Passive Interrogate is initiated by the B300 which, after reading the "M" and "N" variants, sends a Sync (ISYL) level and turns clock control over to the B249 (DTCU). The DTCU recognizing ISYL leaves its Idle state (P = 0 · Q = 0) and goes through a SYNC operation sending ISYL to all CTU's. This action will take place regardless of the condition of the Interrupt Flip-flop in the B249. When any CTU is Read-Ready, the number of the CTU along with the control level IRRL (Inquiry Read-Ready) and the timing level ITCL (Inquiry Time for Character) will be passed along to the B300.

When no Interrupt condition exists only the timing level ITCL will be sent to the Processor.

The B300 recognizing ITCL will check IRRL (Inquiry Read-Ready). If there is no CTU Read-Ready, the B300 will proceed directly to CUF = 15 ending the instruction. If however, there is a CTU Read-Ready, the B300 will store the number of the Read-Ready CTU in the location pointed to by BBB and will then take the AAA branch.

After the B300 has utilized all the information made available by the B249, the B249 will be released and will return to its Idle state.

DETAILED DESCRIPTION

B300 Operation

CUF = 2 · MCF = 0

Refer to Figure II-20.

The "N" variant which should be zero is read and placed into the SCF's.

CUF = 1 . MCF = 0

The "M" variant which should be one is read and placed in the MVF's.

DI8F will be set if there is NO CTU Read-Ready (SIIL/).

CUF = 1 · MC3F

The logic to set CUF = 15 when DI8F (no Interrupt) is on should be disabled with a CTU (B486) is in use.

The CP will Idle until there are no card operations in progress (CCNL/) at which time SC7F is set. With SC7F and the B249 Ready (ISRL), the following actions take place:

1. SCF → CIF - The "N" variant, which is zero, is sent to the DTCU.
   CIF → ØInL
2. Set ISYL - DI1F is set sending ISYL to the DTCU.
3. Set SYNF - Turn clock control over to the DTCU. Clear RUNF

The B300 will now await a response from the DTCU.

DTCU Operation

Refer to Figure II-9.

P = 0 · Q = 0 (A-clock)

When ISYL (Inquiry Sync) arrives from the B300, an "A" clock pulse is produced setting Q2F.

P = 0 · Q = 2 + 3 (A-clock)

The "A" clock remains enabled by ISYL.

The only actions to take place when the "A" CLP occurs are to set P = 4 and Q = 0.

P = 4 . Q = 0 (B-clock)

Refer to Figure II-10 (Page 1 of 2).

The CTU causing the interrupt or the TU last receiving System attention is checked for Unit Ready. If the TU is Ready, BQF is set.

P = 4 · Q = 0 (A-clock)

When the "A" CLP occurs, BQF is checked and when found on (TURL) results in P = 4 · Q = 1. If BQF is found off (TURL/) "P" is left at 4 while "Q" is set to 3 bypassing Q = 1. This action is necessary because P = 4 · Q = 1 depends on a Timing pulse from the addressed CTU.

P = 4 · Q = 1 (A-clock)

Refer to Figure II-10 (Page 2 of 2).

The "A" clock is enabled by TCTL (Terminal Character Time) from the designated CTU. TCTL is generated by a CTU any time it is designated and is at Order = 1 and P = 0.

With the "A" clock, the status and type of the designated Terminal Unit are staticized into the "R" and "T" registers respectively.

The significance of the "R" register is;

R4F - TU is Write-Ready

R3F - TU is Read-Ready

R2F - TU is Busy

R1F - TU is Not Ready

The "P" register remains at four while Q is SET to three.

P = 4 · Q = 3 (B-clock)

There will be two "B" clock pulses produced, one when ATDM times out and the other one 7μs later.

The first "B" CLP will place the contents of the "S" register (TU#) into the "B" register and therefore on the information lines to the Processor. This clock pulse will also RESET AQF, set BQF and trigger the 4μs multi BTDM. With BTDM ON and AQF OFF, ITCL (Inquiry Time for Character) is sent to the B300 allowing a CCP to be produced. AQF = 0 is gated into this logic to allow a half microsecond for the information lines to settle down.

The "B" clock remains enabled by the logic AQF = 0 and BQF = 1. Therefore, the next "B" clock pulse will occur in the minimum time of 7μs and will RESET BQF.

P = 4 · Q = 3 (A-clock)

The DTCU will wait at this point until the B300 has completed its operation at which time ISYL = 0 (DI1F/) will allow the "A" clock pulse to occur. This "A" CLP will clear "P" and "Q" returning the DTCU to its Idle state.

B300 OPERATION

Refer to Figure II-20.

CUF = 1 · MC3F

ITCL arriving from the DTCU will produce one CCP which will SET RUNF placing the B300 on its own clock. At this time DI8F is checked and if it is found OFF, signifying an Interrupt condition (CTU Read-Ready) exists, CUF will be SET to 8 while the number of the CTU causing the interrupt is placed in the AIF. If DI8F is found ON, CUF cannot be set to 8 and will therefore be SET to 15 completing the instruction. CUF could not be set to 5 or 11 at this time because MV8F is not on. MV8F at this point denotes an Active Interrogate which is not normally used with CTU operation.

CUF = 8,7,6 · MCF = 0

The BBB address is read and placed in MAR.

CUF = 6 · MCF = 0

While the hundreds digit of the BBB address is being placed in the MHF's the CTU number is transferred from AIF and CIF.

CUF = 6 · MC2F

The number of the Read-Ready CTU is stored in the location pointed to by BBB.

Since the CTU must be Read-Ready, the term IWRL/ (Inquire Write-Ready Not) will be true causing CUF to be SET to 5. The B300 will now go through CUF 5, 4 and 3 and then 14, resulting in the AAA branch.

At CUF = 14 DI1F will be cleared sending ISYL/ to the DTCU allowing it to go back to its Idle state.

B300 READ - ITU (B486) MODE

OP = L = 35

M = 2 Read to Group Mark

10 Read Ignore Group Mark - Should NOT be used with CTU.

N = Unit designate - numeric bits only. Zone bits must be OFF.

AAA = Branch to when Designated Terminal is Not Ready.

BBB = Branch to when Designated Terminal is Not Read-Ready.

CCC = Points to MSD position of input field.

GENERAL DESCRIPTION

Refer to Figure II-28.

The Read Instruction will transfer the contents (87 characters plus GM) of a buffer in the CTU designated by the "N" variant into the field pointed to by CCC. When the designated CTU is Not Ready, the AAA Branch will be taken. When the designated CTU is Unit Ready but not Read-Ready, the BBB branch will be taken.

The Read operation is initiated by the B300. After the B300 has completed its preliminary steps, read M, N and CCC, it sends the number of the CTU to be read along with the control levels ISYL (Inquiry Sync) and RINL (Read Inquiry) to the DTCU.

The B249 (DTCU) recognizing ISYL will proceed from its Idle state P = 0 · Q = 0 to P = 0 · Q = 2 where the number of the CTU to be read is accepted into the "S" register. Because RINL indicates this is a read operation, the DTCU will go to P = 5 · Q = 0 where the ready condition of the Designated CTU is checked. If the CTU is indeed ready the DTCU will proceed to P = 5 · Q = 1 where the CTU status (should be Read-Ready) and type are staticized into the "R" and "T" registers respectively. The CTU provides a timing level (TCTL) which allows the DTCU to go on to P = 5 · Q = 3.

At P = 5 · Q = 0 when the designated CTU is found Not Ready (TURL/) the DTCU will bypass P = 5 · Q = 1 and will go directly to P = 5 · Q = 3.

During P = 5 · Q = 3 the DTCU will send the CTU number back to the B300 accompanied by the timing pulse ITCL (Inquiry Time for Character). At the B300 the CTU number is placed in the AIF's while the NVF's are counted from zero to one. This CTU number in the AIF's is of no significance and will be discarded when the first information character arrives.

The DTCU having sent one timing pulse (ITCL) to the B300 now proceeds to P = 1 · Q = 0 and thence to P = 1 · Q = 1 where it will remain for the entire information transfer.

The DTCU now sends ICTL (Inquiry Character Time) to the CTU. The Designated CTU (TUDS) recognizing ICTL proceeds for its Idle state (Ø = 1 · P = 0) through Ø = 1 · P = 2 to Ø = 5 · P = 0 where the Address portion of scratchpad is read and then to Ø = 5 · P = 1. At this point the Information transfer begins.

Functional Detail

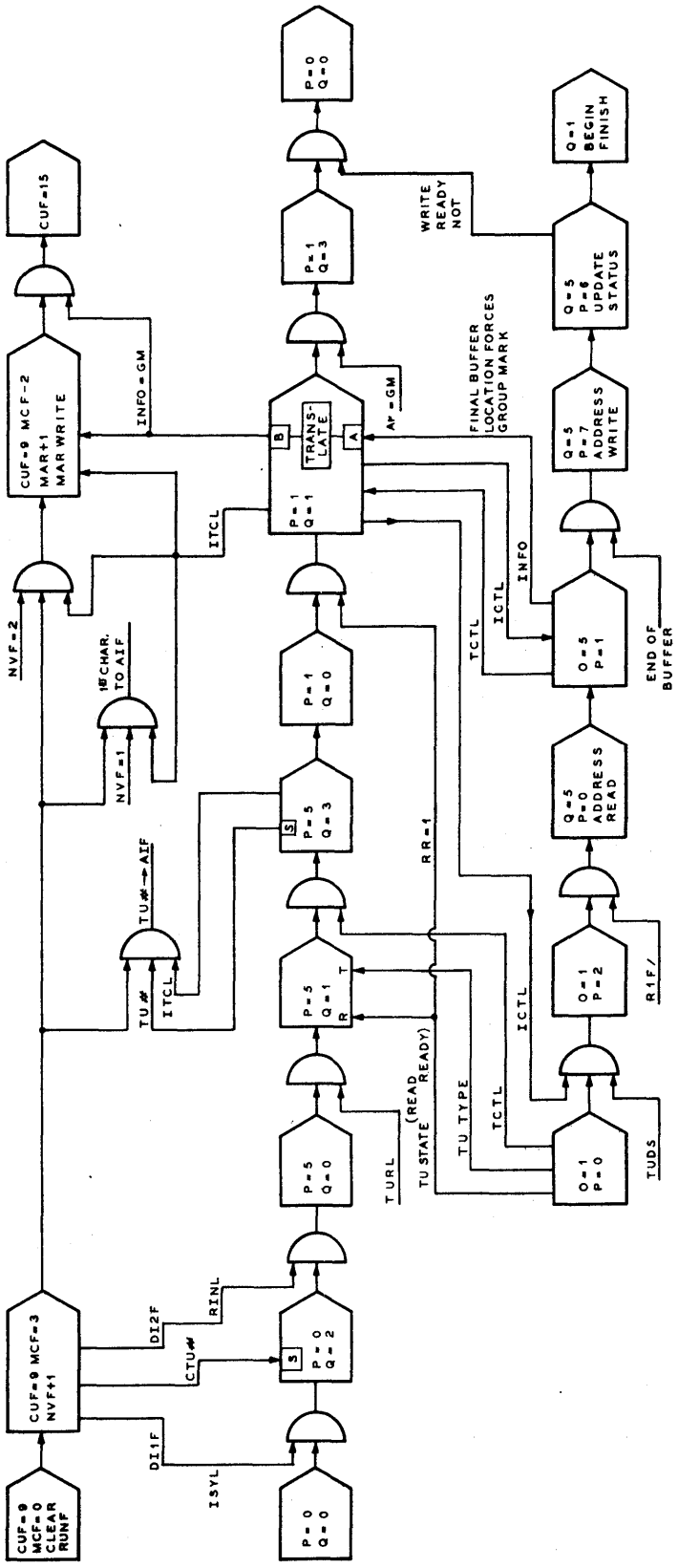


FIGURE II-28
ITU READ - BLOCK FLOW

The CTU reads a character and places it on the information lines to the DTCU accompanied by the timing level TCTL (Terminal Character Time). The DTCU will accept the Character into its "A" register from whence it is sent through the translator to the "B" register. As soon as the DTCU accepts a character into the "A" register, it will send ICTL to the CTU requesting another. When a character has been transferred from "A" to "B", the DTCU will place the next character from the CTU into "A". When a character arrives in the "B" register, it is on the information lines to the Processor accompanied by ITCL (Inquiry Time for Character).

When the first information character arrives at the B300, it will be placed into the AIF while NVF will be counted from one to two. When the second character arrives, it will be placed into the AIF while the first character is transferred from AIF to CIF. At this time NVF will be found equal to two causing the Processor to go to CUF = 9· MC2F where character number one is stored in memory. As each character arrives at the B300 it is placed in the AIF while the preceeding character is placed in CIF and stored.

This process continues until the CTU reaches its Final Buffer Location at which time it forces a Group Mark over to the DTCU. After the DTCU has accepted the GM, the CTU goes through Ø = 5 · P = 7 to Ø = 5 · P = 6 where its status is changed from Read-Ready to Write-Ready therefore sending Read-Ready not to the DTCU. The CTU has now completed the read and goes back to Ø = 1 and P = 0.

After the DTCU has sent the GM to the B300, the DTCU goes to P = 1 · Q = 3 and, when the CTU has changed its state the DTCU goes back to P = 0 · Q = 0.

The B300 recognizes the GM on the Information lines at which time it goes back on Processor clock. After the GM has been stored, the Processor will go to CUF = 15 completing the Read operation. Refer to Figure II-28.

DETAILED DESCRIPTION

B300 Operation

Refer to Figure II-23 and II-31.

CUF = 2 · MCF = 0

The "N" variant which is the CTU number is read and placed in the SCF. The CTU number is represented by the numeric bits. The zone bits must be zero.

CUF = 1 · MCF = 0

The B300 may Idle at this point allowing BAPL until there are no card cycles in progress (CCNL/) at which time SC7F is SET. With SC7F ON and the B249 (DTCU) Ready, CUF is set to 11. If the DTCU is found Not Ready, CUF will not be set to 11 and CEF will be cleared.

CUF = 11,10,9 · MCF = 0

The CCC address is read and placed in MAR.

CUF = 9 · MCF = 0

In addition to the hundreds digit of the CCC address being placed in MAR, the following actions take place:

1.	SCF → CIF CIF → ØInL	Transfer the CTU number fo the CIF and thence to the B249 on the output information lines.
2.	SET ISYL	Set DI1F which sends ISYL to the DTCU.
3.	SET SYNF Clear RUNF	Turn clock control over to the DTCU.
4.	SET RINL	Set DI2F which sends RINL to the DTCU.

CUF = 9 · MC3F

The B300 now awaits a response from the DTCU.

DTCU Operation

P = 0 · Q = 0 (A-clock)

Refer to Figure II-9.

ISYL arriving from the B300 produces an "A" clock pulse which SETS Q2F.

P = 0 · Q = 2 + 3

The "A" clock is enabled by ISYL. The number of the CTU to be read is on the information lines from the B300 and is placed in the "S" register. Note that this logic is enabled by [ITU = MODE pluggable] = 1. This term will come true because the zone bits on the information lines are equal zero. Since RINL (Read Inquiry) is being sent from the B300, "P" is SET to 5 while "Q" is cleared.

P = 5 · Q = 0 (B-clock)

Refer to Figure II-10 (Page 1 of 2).

The "B" clock pulse will occur when ATDM times out. The Designated CTU is checked for Power ON and Remote (TURL). If it is ready, BQF is SET and if it is Not Ready BQF is left reset. In either case AQF is RESET.

P = 5 · Q = 0 (A-clock)

The "A" clock is enabled by AQF = 0 and will occur at the minimum 7μs. If BQF is found ON (TURL), "Q" will be SET to 1. If BQF is found OFF (TURL/), "Q" will be SET to 3.

This action is necessary because P = 5 · Q = 1 depends on a Timing pulse (TCTL) from the CTU.

P = 5 · Q = 1 (A-clock)

Refer to Figure II-10 (Page 2 of 2).

The "A" clock is enabled by TCTL (Terminal Character Time) from the CTU. This level is produced any time a designated CTU is at Ø = 1 and P = 0.

When the "A" CLP occurs the status of the designated CTU is placed into the "R" register while the type of Terminal is placed into the "T" register to enable the proper translation. The status lines reflects the condition of the "R" register in the CTU which should be equal to 3 or 6 sending the Read-Ready level to the DTCU. This will cause R3F in the DTCU to be SET. The type lines from the CTU will cause "T" to be SET to 2 resulting in ASCII to BCL translation when the information transfer takes place. AQF is SET and BQF is RESET.

P = 5 · Q = 3 (B-clock)

There will be two "B" clocks produced. The first occurs when ATDM times out. With the first "B" clock, the CTU number is transferred from "S" to "B" and then to the B300. The status of the CTU is sent to the Processor as reflected by the DTCU "R" register. At this point IRRL (Inquiry Read-Ready) should be produced by R3F. BTDM is triggered and AQF is RESET sending ITCL (Inquiry Time for Character) to the Processor. AQF is gated into this logic to provide an 0.5μs delay to allow the information lines time to settle down. BQF is SET.

The second "B" clock pulse is caused by AQF = 0 · BQF = 1 and will occur in the minimum 7μs. This "B" CLP simply clears BQF to provide enabling logic for the "A" clock.

P = 5 · Q = 3 (A-clock)

The "A" clock pulse will occur when the B300 sends ISYL = 0 signaling that it is ready to start the information transfer. When the "A" CLP occurs, "P" will be SET to one if the CTU is Read-Ready (R3F) and "Q" will be cleared. If the CTU was Not Read-Ready, R3F will be found OFF causing "P" to be cleared returning the DTCU to its Idle state.

B300 Operation

CUF = 9 · MC3F

Refer to Figure II-23.

ITCL (Inquiry Time for Character) arriving from the DTCU fires the clock B0 producing one CCP.

The Status of the designated CTU is now checked. If it is Not Ready (TURL/), CUF is set to 5 and the AAA branch is taken. If the CTU is

Unit Ready but Not Read-Ready, CUF is SET to 8 and the BBB branch is taken.

When the CTU is Unit-Ready and Read-Ready the MVF's are counted from 0 to 1 and the Buffer number being sent from the DTCU on the INnL lines is gated into the AIF but is of no significance. DI1F is RESET sending ISYL/ to take DTCU. The Processor is now at CUF = 9 · MC3F · NVF = 1 · RUNF/ awaiting the first Information character to be sent from the DTCU.

B249 Operation

P = 5 · Q = 3 (A-clock)

Refer to Figure II-10 (Page 2 of 2).

When ISY = 0 arrives from the B300 an "A" CLP will be generated. With the "A" CLP,R3F is checked. If R3F is found OFF, the CTU is Not Read-Ready. Therefore, the operation is complete and the DTCU returns to P = 0 · Q = 0. If R3F is found ON, the CTU is Read-Ready and the Information transfer will take place. In this case "P" is SET to one while "Q" is cleared.

P = 1 · Q = 0 (A-clock)

Refer to Figure II-11.

The "A" clock pulse SETS Q = 1.

P = 1 · Q = 1 (A-clock)

ICTL (Inquiry Character Time) is sent to the CTU. The "A" clock will be enabled when the CTU signals that it has the first character available by sending TCTL (Terminal Character Time).

B486 Operation

The System Read operation is initiated in the CTU at Ø = 01 · P = 0 when ACANS/ indicates that none of the channels require attention. ICTS indicates that the DTCU and Central Processor are ready to receive information. R3F indicates that the CTU is System Read-Ready, and TUDS indicates that the DTCU Scanner has located this CTU.

Ø = 01 · P = 2

Refer to Figure II-29.

The channel number is transferred from the "T" to the "S" register with SFTS. Order is set to 05, and "P" is cleared.

Functional Detail

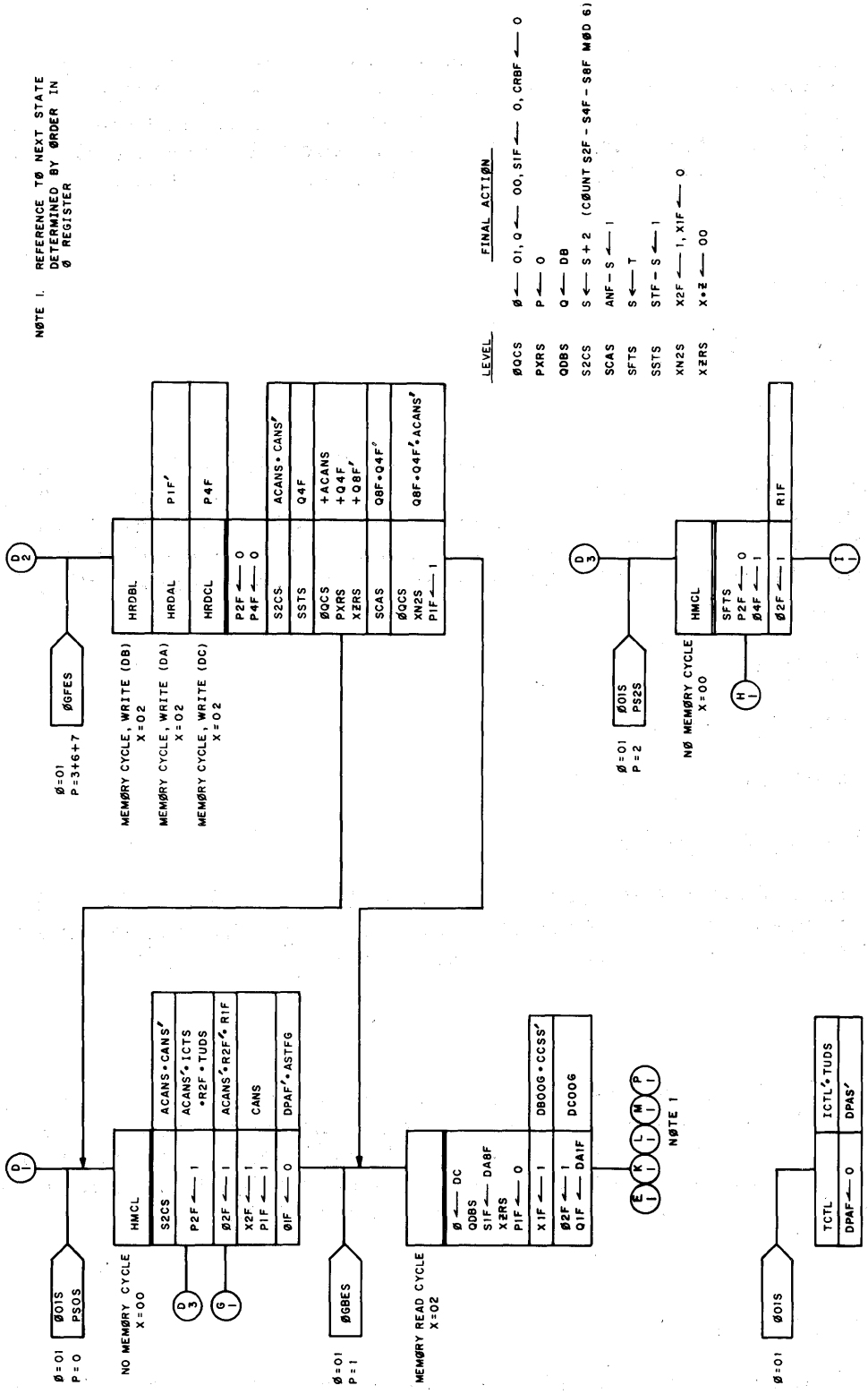


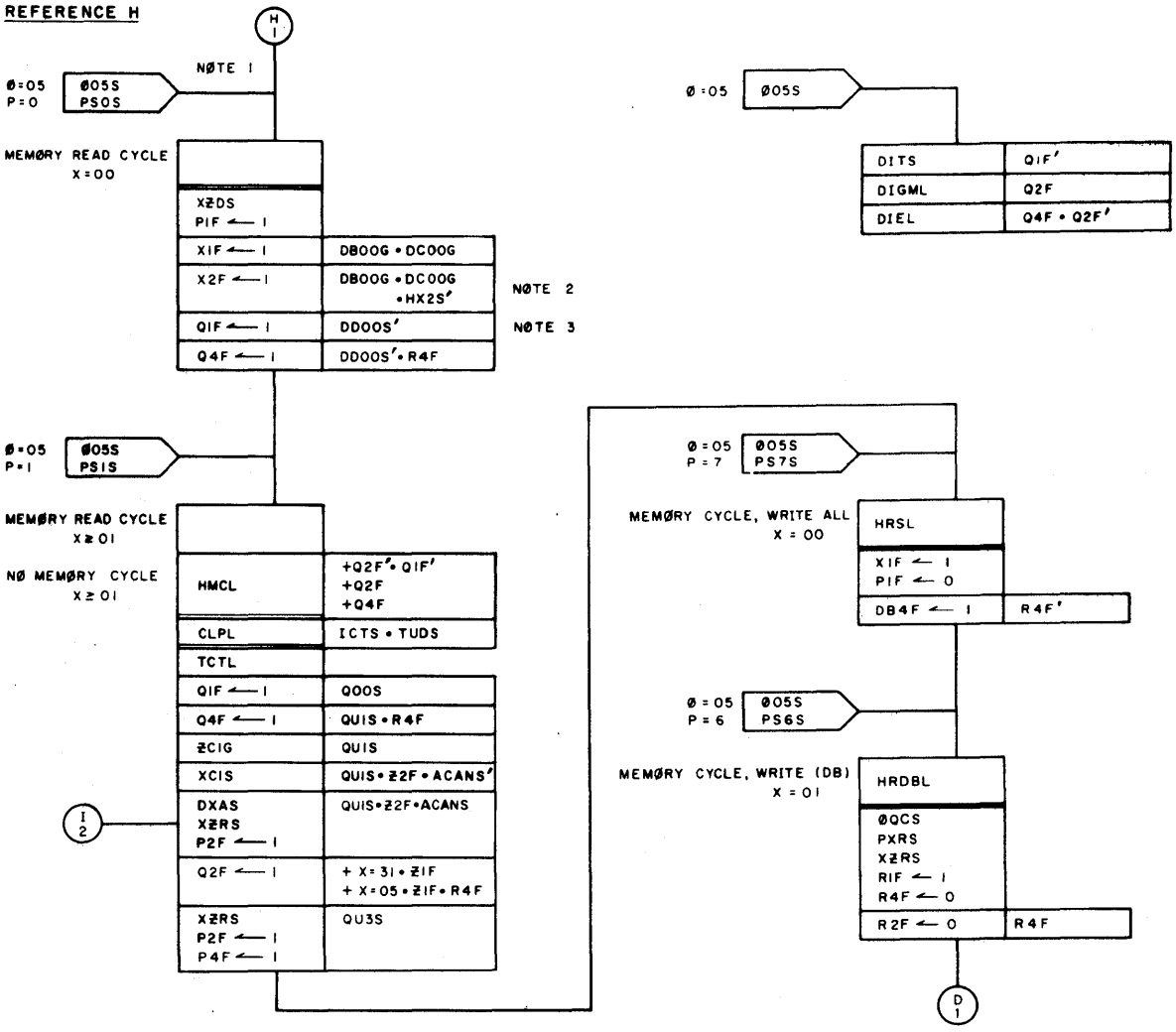
FIGURE II-29
BEGIN & FINISH FLOW

Functional Detail

Ø = 05 · P = 0 · X = 03

Refer to Figure II-30.

The Address cell of Scratchpad is read into the "DB" and "DC" registers.



LEVEL	FINAL ACTIØN
DIEL	DI ← 14 (NØ CLØCK)
DIGML	DI ← 15, TRBL' ← 1 (NØ CLØCK)
DITS	DI ← T (NØ CLØCK)
DXAS	DB • DC ← X • Ƶ + 1
ØQCS	Ø ← 01, Q ← 00, SIF ← 0, CRBF ← 0
PXRS	P ← 0
XCIS	X ← X+1
XƵDS	X • Ƶ ← DB • DC
XƵRS	X • Ƶ ← 00
ƵCIG	Ƶ ← Ƶ+1 (MØD 3)

NØTE 1. R=2 OR R=6 DURING ALL ØF Ø=05

NØTE 2. HX2S' HERE DENØTES R4F'

NØTE 3. DDOOS' DENØTES [DBOOG•DCOOG]'

FIGURE II-30
READ TO DTCU FLOW

The "X" register is set to 03 when the "DB" and "DC" registers equal zero. This signifies that the Input message to System is being initiated and it is NOT an Error message (HX2S/).

Ø = 05 · P = 1 · X = 03

Q1F/ and Q2F/ inhibits a Memory cycle at this time because DITS is gating the buffer number from the "T" register via DI to the DTCU (TR lines). After the buffer number is in the DTCU "A" register, it requests another character by returning ICTS to this CTU (TUDS).

A Clock Pulse is generated to step "Q" to 01 and initiates a Memory cycle. The "TC" number is read from the first Information cell and sent to the DTCU from the "DA" register via the DI switches. The CTU idles until DTCU requests another character by returning ICTS after the "TC" number is in the DTCU "A" register. Each Clock Pulse counts "Z" from this point on to select the character that is to be sent to the System from the "DA", "DB" or "DC" registers.

Z = 0	DA to DI to TR
Z = 1	DB to DI to TR
Z = 2	DC to DI to TR

The CTU remains at this "P" count in this Order while three Memory cycles are executed at each Address to bring the Information into the "D" register and then gate the three characters into DI as shown above. The "X" register is counted to address the next Information cell when Z = 2 indicates that three characters have been read from this cell. The "Z" register is counted and three Memory cycles are executed at this Address with each ICTS to send the proper character from the "D" register to the DTCU until this cell is completely read.

The operation continues until Q2F is set by X = 31 and Z1F indicating that the entire buffer has been read. This forces a Group Mark into the DI switches with DIGML. The Group Mark is accepted by the DTCU and the next clock pulse generated with the ICTS returned from the DTCU SETS "P" to 7 and clears the "X" and "Z" registers.

Ø = 5 · P = 7

The Parity/Address cell is cleared with the Memory Write cycle. The "X" Register is SET to 01 and "P" is SET to 6.

Ø = 5 · P = 6

The Write from DB retains the System Status bits (DB4F) in Scratchpad. ØQCS SETS Ø = 01, "P" is cleared, the "X" and "Z" registers are cleared, and the "R" register is SET to 3 to indicate that the CTU is System Write Ready.

B249 Operation

P = 1 · Q = 1 (A-clock)

Refer to Figures II-11 and II-31.

Functional Detail

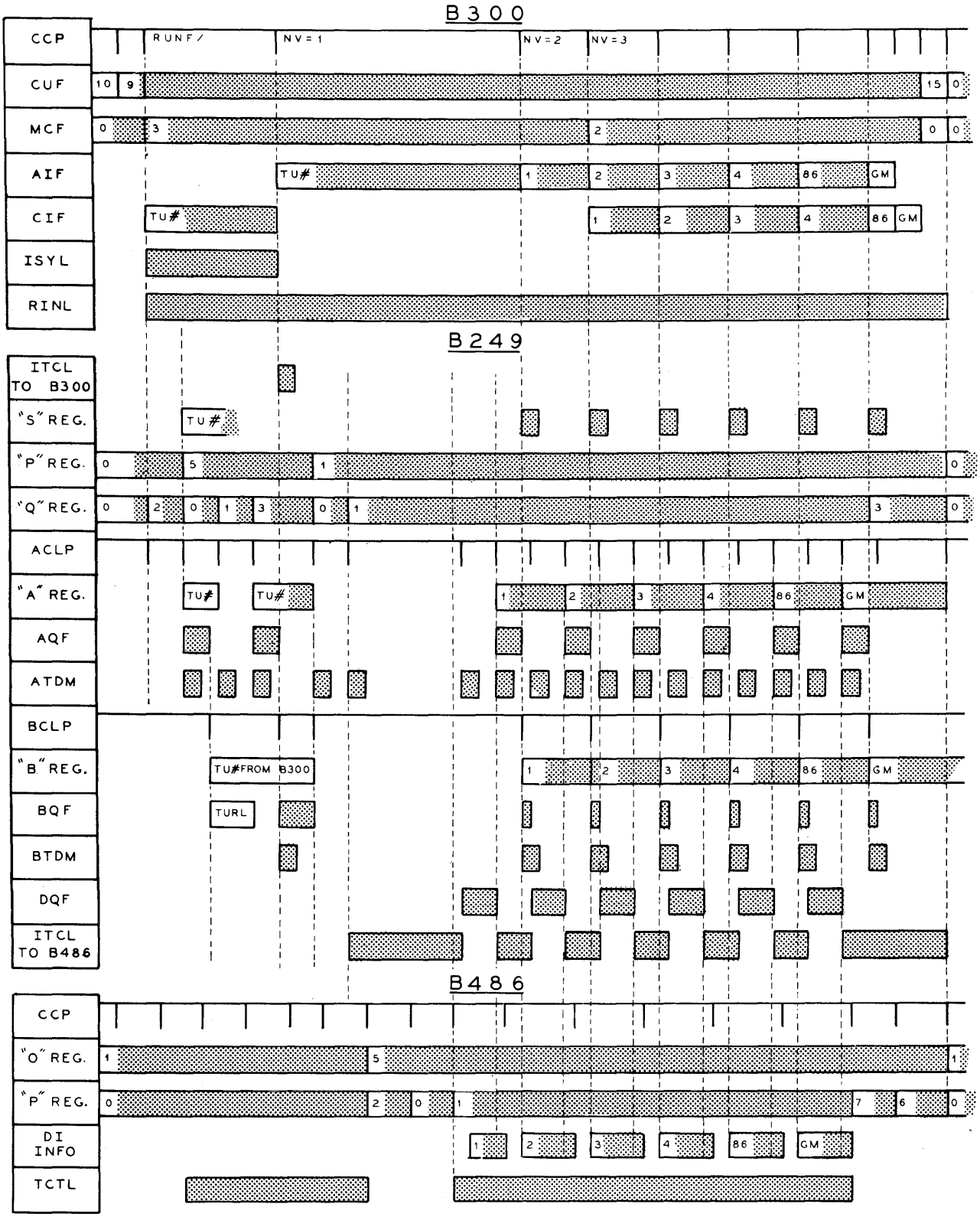


FIGURE II-31
ITU READ TIMING

The CTU sends TCTL (Terminal Character Time) to the DTCU when it has the first character available. Since TCTL will remain true for the entire information transfer, the "A" clock will free run at its 7μs rate. The first "A" CLP SETS DQF disabling ICTL to the B486. The next "A" CLP accomplishes the following:

1. Place the character into the "A" register.
2. Set AQF marking "A" occupied.
3. Trigger ATDM.
4. Reset DQF sending ICTL to the CTU requesting the next character.

P = 1 · Q = 1 (B-clock)

The "B" clock pulse is produced when ATDM times out and will therefore occur prior to the next "A" clock.

The "B" clock will;

1. Transfer a character from the encoder outputs of the translator into the "B" register from whence it is placed on the information lines to the Processor.
2. Set BQF marking "B" occupied.
3. Reset AQF marking "A" unoccupied.
4. Trigger BTDM to send ITCL to the Processor. Note that BTDM RESETS BQF.

P = 1 · Q = 1 (A-clock)

The next "A" CLP will again SET DQF disabling ICTL to the B486. The second "A" CLP in this sequence will;

1. Place a character in "A".
2. Set AQF marking "A" occupied.
3. Trigger ATDM.
4. Reset DQF sending ICTL to the B486.

P = 1 · Q = 1 (B-clock)

The "B" CLP occurs when ATDM times out and will;

1. Transfer a character into "B".
2. Set BQF.
3. Reset AQF.
4. Trigger BTDM to send ITCL to the B300.

This process continues until a "B" clock transfers the Group Mark into the "B" register at which time "Q" is SET to 3.

P = 1 · Q = 3 (A-clock)

After the CTU has changed its state to Write-Ready, an "A" clock will clear "P" and "Q" completing the Read operation.

B300 Operation

CUF = 9 · MC3F

Refer to Figure II-23.

The NVF was stepped to 1 during the SYNC. This occurred when the DTCU sent the CTU number and ITCL. This CTU number is in the A1F, but is of no significance.

After the DTCU has the first character to be stored on the INnLs, it provides ITCL for the Processor. ITCL fires the Clock B0 providing a CCP.

The NVF's are now stepped to 2 and the first character is placed in the AIF's. When the second character is available from the DTCU, ITCL once again provides a CCP for the Processor. Because NV2F is now found ON, the first character being held in the AIF's is transferred to the CIF's and the MCF's are SET to 2 initiating a MAR write to store the first character while the second character is transferred from the INnL's to the AIF's.

CUF = 9 · MC2F

Each ITCL provides a CCP which will;

1. Transfer a character from AIF to CIF.
2. Count MAR + 1.
3. Initiate a MAR Write to store that character.
4. Place a new character in the AIF.

This process will continue until the complete message has been transferred to the Processor as signified by the arrival of the GM on the INnL's.

When this situation occurs, the Group Mark will be placed in the AIF and RUNF will be turned ON. The Processor is back on its own Clock. The next CCP will transfer the Group Mark to the CIF's and will initiate a MAR Write to store that character. This CCP finding RUNF ON, will clear SYNF and SC7F. The next CCP will occur after the Group Mark has been stored and will find SC7F/. This will provide the logic to SET CUF = 15 and MCF to zero to exit this instruction.

B300 WRITE - ITU (B486) MODE

OP = L = 35

M = 4 Write to Group Mark

12 Write and Ignore Group Mark. Should not be used with CTU.

N = Unit Designate. Numeric bits only. Zone bits must be OFF.

AAA = Points to MSD position of Output Field.

BBB = Branch to when designated. Terminal is not Write-Ready.

CCC = Branch to when designated. Terminal is Not-Ready.

GENERAL DESCRIPTION

Refer to Figure II-32.

The Write instruction will transfer information from the field pointed to by AAA in the B300 to a Buffer in the CTU designated by the "N" Variant. The transfer will be terminated by a Group Mark or by reaching the end of the CTU Buffer (Buffer Final Location (88 characters).

When the designated CTU is found not ready, the CCC branch will be taken. When the designated CTU is found Unit-Ready but not Write-Ready, the BBB branch will be taken.

The Write operation is initiated by the B300. After the B300 has completed its preliminary steps (Read M, N and AAA), it sends the number of the CTU to be written to along with the Control Levels ISYL (Inquiry Sync) and WIRL (Write Inquiry) to the DTCU (B249).

The B249, recognizing ISYL, will proceed from its Idle state P = 0 · Q = 0 to P = 0 · Q = 2 where the number of the CTU to be written to is placed in the "S" Register.

Because WIRL signifies this is a Write operation, the DTCU will go to P = 6 · Q = 0 where the Ready condition of the CTU is checked. When the CTU is found Ready, the DTCU will proceed to P = 6 · Q = 1 where the CTU status (should be Write-Ready) and type are staticized into the "R" and "T" Registers respectively. The CTU provides a timing level (TCTL) which allows the DTCU to go onto P = 6 · Q = 3.

At P = 6 · Q = 0, when the designated CTU is found Not-Ready (TURL/), the DTCU will by-pass P = 6 · Q = 1 and will go directly to P = 6 · Q = 3.

During P = 6 · Q = 3, the DTCU will send the status of the designated CTU (IWRL) back to the B300 accompanied by the Timing pulse ITCL (Inquiry Time for Character). The CTU number ("S" Register) is also

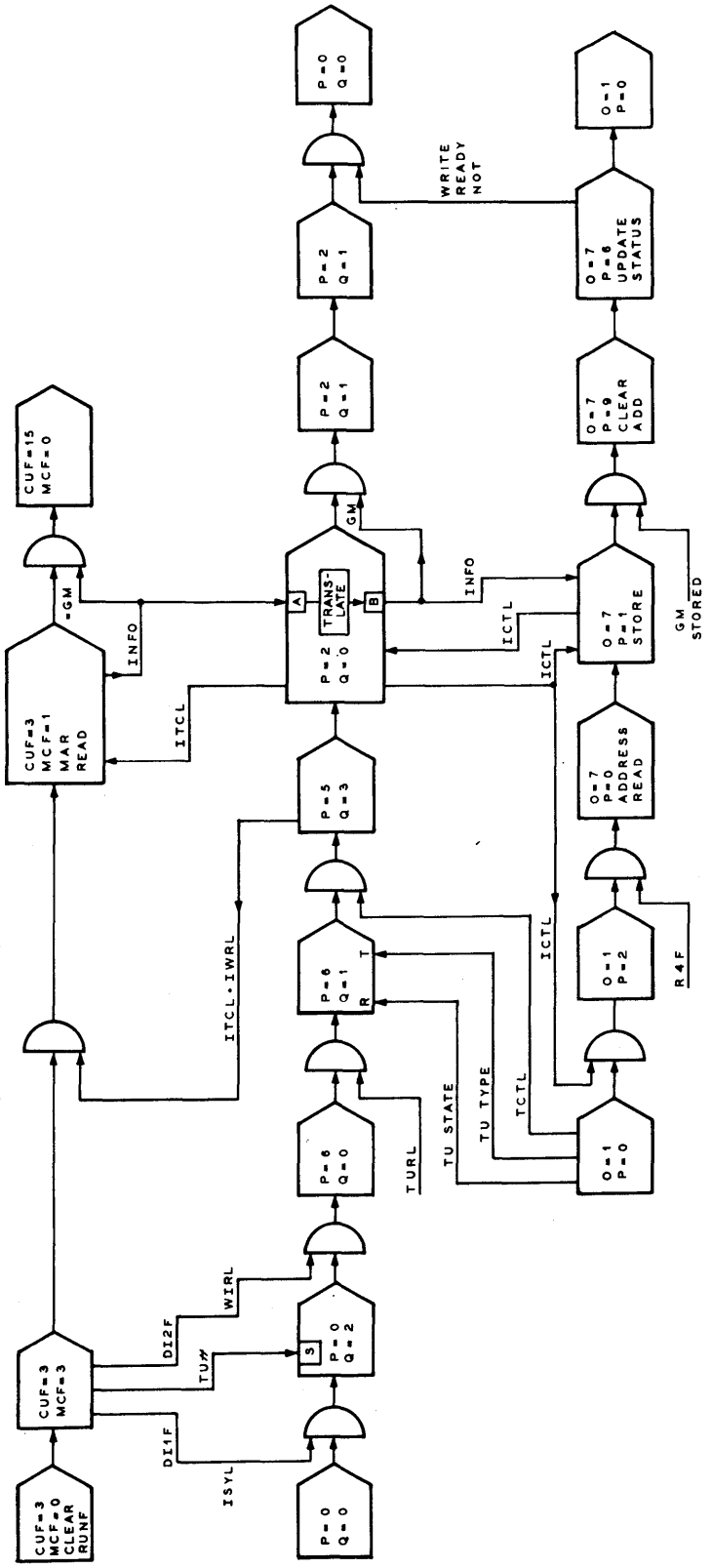


FIGURE II-32
ITU WRITE - BLOCK FLOW

sent but is of no significance.

The Processor, receiving ITCL and IWRL, proceeds to CUF = 3 and MC1F where the first character to be transferred is read and placed on the information lines. Also at this time, ISYL/ is sent to the DTCU.

With the arrival of ISYL/, the DTCU proceeds to P = 2 · Q = 0 where;

1. The first character is placed into the "A" Register and is transferred to the "B" Register via the Translator. When the character reaches "B", it is on the information lines to the CTU.
2. ITCL is sent to the Processor requesting the second character.
3. After the second character reaches the "A" Register, the DTCU sends ITCL to the Processor requesting the third character.

At this point, the CTU will be brought into Sync and no further information will be requested from the Processor until after the CTU accepts the first character.

The DTCU sends ICTL to the CTU to inform it that the Information Transfer is to take place.

The designated CTU (TUDS), recognizing ICTL, leaves its Idle state (Ø = 1 · P = 0) and goes through Ø = 1 and P = 2 to Ø = 7 · P = 0 where the Address portion of Scratchpad is read. From here, the CTU goes to Ø = 7 · P = 1 and accepts the first character to be stored. After accepting the character, the CTU sends TCTL (Terminal Character Time) to the DTCU.

The DTCU recognizing TCTL will transfer a character from "A" to "B" and then to the CTU. Accompanying the character to the CTU will be the Timing pulse ICTL, which informs the CTU that a new character is available.

As soon as the "A" Register is unoccupied, the DTCU will place the character on the Information lines from the Processor into "A". The DTCU will then send ITCL (Inquiry Time for Character) B300 requesting the next character.

This process continues until the character being transferred is a Group Mark or until the Final Location of the CTU Buffer is filled.

When either of these conditions occur, the Processor will exit the instruction. The DTCU recognizing either GM or IFAL (Inquiry Final Address) will proceed through P = 2 · Q = 1 to P = 2 · Q = 3 where it waits for the CTU to change its state from Write-Ready to Not-Write-Ready (Idle).

After the CTU has stored the Final character or Group Mark, it goes to Ø = 7 · P = 7 to clear ADD, and then on to Ø = 7 · P = 6 to update its status.

It is at this point that the CTU informs the DTCU that it is no longer

Write-Ready. The final CTU action is simply to return to its Idle state (Ø = 1 · P = 0).

When the DTCU becomes aware that the CTU is no longer Write-Ready, it returns to its Idle state (P = 0 · Q = 0) and the operation is complete.

DETAILED DESCRIPTION

B300 Operation

Refer to Figure II-26.

CUF = 2 · MCF = 0

The Numeric portion of the "N" variant which specifies the CTU to be written to, is placed in SCF 1-4. The Zone bits in the "N" Variant must equal zero and will, therefore, clear SCF5 and 6.

CUF = 1 · MCF = 0

The "M" Variant is read and placed in the MVFs. The 4-bit must be ON for a Write instruction. The 8-bit ON, denotes Ignore-Group-Mark and should not be used in ITU mode.

CUF = 1 · MC3F

The B300 now allows BAPL until all Card Cycles have been completed, at which time CCNL/ SETS SC7F as a SYNC. SC7F in turn SETS CUF to 5 and clears MCF.

CUF = 5,4,3 · MCF = 0

The AAA Address which points to the MSD position of the field to be written, is read and placed in MAR.

CUF = 3 · MCF = 0

While the Final digit of the AAA Address is being placed in MAR, the following actions take place:

1. SCF → CIF - Place the CTU number into CIF.

   CIF → OInL - Output Information Lines. Note that the transfer of CIF to OInL is binary. This is necessary because internal zero would translate to a BCL 10 which would confuse the DTCU.

2. SET ISYL - The actual logic here is to SET DI1F which sends ISYL (Inquiry Sync) to the DTTU.

3. SET WIRL - DI4F is SET and sends WIRL (Write Inquiry) to the DTCU.

4. SET SYNF - Turn Processor Clock Control over to the DTCU and clear RUNF.

At this point, the B300 waits for the DTCU to SYNC.

B249 DTCU

P = 0 · Q = 0 (A-clock)

Refer to Figure II-9.

The "A" clock is enabled (ACL) by ISYL arriving from the B300. When the "A" clock pulse occurs, Q2F is SET. It is possible that Q1F could also be SET if a Scan Cycle is in progress (SCA = 1).

P = 0 · Q = 2 + 3 (A-clock)

The "A" clock remains enabled (ACL) by ISYL.

The number of the CTU to be written to is on the Information lines from the B300 and is placed into the "S" Register. Note that this logic is enabled by [ITU - Mode Pluggable] = 1. This term will come true because the zone bits on the Information lines are equal zero.

Since a Write operation is being called for the B300 will send WIN (Write Inquiry) to the DTCU. This will cause "P" to be SET to 6 while "Q" is cleared.

P = 6 · Q = 0 (B-clock)

Refer to Figure II-10 (Page 1 of 2).

The "B" Clock pulse will occur when ATDM times out. The designated CTU is checked for Power ON and Remote (TURL). If it is Ready, BQF is SET and if it is Not-Ready, BQF is left RESET. In either case, AQF is RESET.

P = 6 · Q = 0 (A-clock)

The "A" Clock is enabled by AQF = 0 and will occur at the minimum 7μs. If BQF is found ON (TURL), "Q" will be SET to 1. If BQF is found OFF (TURL/), "Q" will be SET to 3.

This action is necessary because P = 6 · Q = 1 depends on a Timing pulse (TCTL) from the CTU.

P = 6 · Q = 1 (A-clock)

Refer to Figure II-10 (Page 2 of 2).

The "A" Clock is enabled by TCTL (Terminal Character Time) from the CTU. This level is produced any time a designated CTU is at Ø = 1 and P = 0. When the ACLP occurs, the status of the designated CTU is placed into the "R" Register while the type of Terminal is placed

into the "T" Register to enable the proper translation.

The status lines reflect the condition of the "R" Register in the CTU which should be equal to 3 sending the Write-Ready level to the DTCU. This will cause R4F in the DTCU to be SET. The type lines from the CTU will cause "T" to be set to 1 resulting in BCL to ASCII translation when the Information transfer takes place. AQF is SET and BQF is RESET.

P = 6 · Q = 3 (B-clock)

There will be two "B" Clocks produced. The first occurs when ATDM times out. With the first "B" Clock, the CTU number is transferred from "S" to "B". However, this is of no significance. The status of the CTU is sent to the Processor as reflected by the DTCU "R" Register. At this point IWRL (Inquiry Write Ready) whould be produced by R4F. BTDM is triggered and AQF is RESET sending ITCL (Inquiry Time for Character) to the Processor. AQF is gated into this logic to provide a .5μs delay to allow the Information lines time to settle down. BQF is SET.

The second "B" Clock pulse is caused by AQF = 0 · BQF = 1 and will occur in the minimum 7μs. This "B" CLP simply clears BQF to provide enabling logic for the "A" Clock.

P = 6 · Q = 3 (A-clock)

The "A" Clock pulse will occur when the B300 sends ISYL = 0 signaling that the first character to be transferred is on the Information lines. When the "A" CLP occurs, "P" will be set to two if the CTU is Write-Ready (R4F) and "Q" will be cleared. If the CTU was Not-Write-Ready, R4F will be found OFF causing "P" to be cleared returning the DTCU to its Idle state.

B300 Operation

CUF = 3 · MC3F

Refer to Figures II-26 and II-33.

ITCL arriving at the Processor, fires the Clock BO providing one CCP. The status of the CTU is now checked for Unit-Ready and Write-Ready. If the CTU is Not-Ready, TURL/ will SET CUF to 11 and SET RUNF. The CCC branch will now be taken. If the CTU is Unit-Ready (TURL) but Not-Write-Ready (IWRL/), CUF will be SET to 8 along with RUNF resulting in the BBB branch.

When the CTU if Unit-Ready and Write-Ready, MCFs will be SET to 1 and the first Memory Read Cycle will be initiated making the first character to be stored in the CTU Buffer available on the ØInLs (Output Information Lines) to the DTCU. Along with this first character, DI1F will be cleared providing ISYL/ to the DTCU.

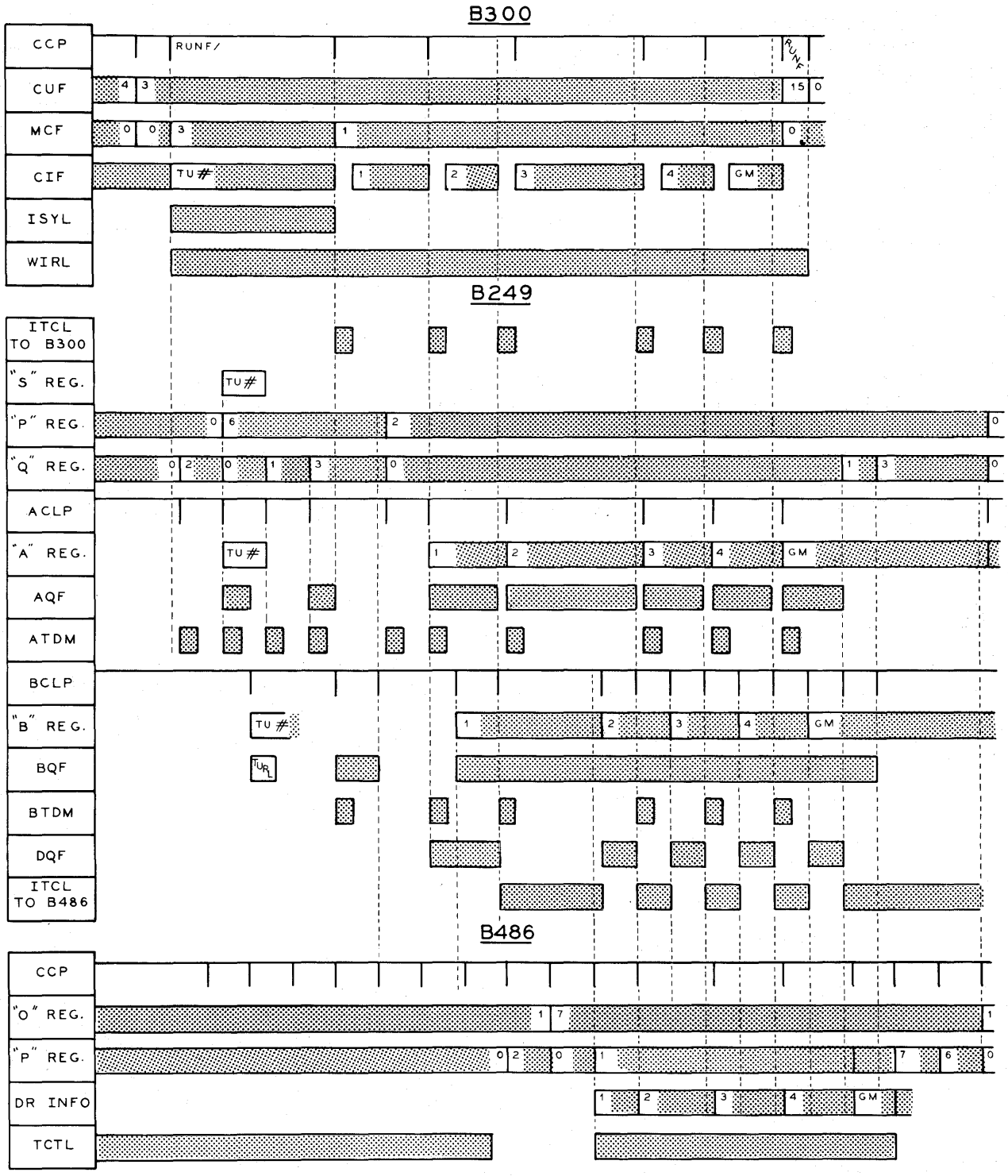


FIGURE II-33
ITU WRITE TIMING

B249 Operation

P = 6 · Q = 3 (A-clock)

Refer to Figure II-10 (Page 2 of 2).

When ISY = 0 arrives from the B300, the "A" CLP will be generated. With the "A" CLP, R4F is checked. If R4F is found OFF, the CTU was Not-Write-Ready. Therefore, the operation is complete and the DTCU returns to P = 0 · Q = 0. If R4F is found ON, the CTU is Write-Ready and the Information transfer will take place. In this case "P" is SET to two while "Q" is cleared.

P = 2 · Q = 0 (A-clock)

Refer to Figure II-12 (Page 1 of 2).

The "A" Clock is enabled by AQ = 0 · WIN = 1 · A≠(111111) · ITU = 1 where;

1. AQ = 0 - AQF is OFF
2. WIN = 1 - The B300 is sending WINL.
3. A≠(111111) - The "A" Register does not contain a Group Mark.
4. ITU = 1 - Pluggable ITU Mode.

When the "A" Clock pulse occurs, the following actions will take place:

1. The first Character is loaded into the "A" Register and AQF is SET.
2. BTDM is triggered to send ITCL to the System requesting the second character. This action is seen under P = 2 Universal state. Note that ATDM is triggered by every "A" Clock pulse.
3. DQF is SET.

The "A" Clock is disabled until AQF is RESET.

P = 2 Universal State

ITCL is sent to the B300 requesting the next character. The type of translation taking place is determined by the "T" Register which is now equal one.

P = 2 · ITU = 1 · BQ = 0 (B-clock)

Refer to Figure II-12 (Page 2 of 2).

The "B" Clock is enabled by AQ = 1 · ATD = 0 · WR = 1 where;

1. AQ = 1 - The "A" Register contains a character.
2. ATD = 0 - Four microseconds have elapsed since the character reached the "A" Register. Therefore, translation is valid.

3. WR = 1 - The CTU is Write-Ready as indicated by its "R" Register.

With the "B" Clock pulse, the character is transferred from the Encoder outputs of the Translator to the "B" Register. BQF is SET marking "B" occupied. Once the character reaches the "B" Register, it is on the Information lines to the CTU.

P = 2 · ITU = 1 · BQ = 1 · DQ = 1 (B-clock)

The "B" Clock pulse will occur in the minimum 7μs and will RESET AQF and DQF.

The situation at this point is;

1. Character number one is in the DTCU "B" Register and is, therefore, on the Information lines to the CTU.
2. Character number two is in the B300 CIF and is on the Information lines to the DTCU.

With AQF and DQF OFF, there are two simultaneous actions to consider:

1. Because AQF is OFF, the "A" Clock is enabled to accept the second character and to send ITCL to the B300 requesting the third character.
2. With DQF OFF, ICTL is sent to the CTU informing it that the first character is available.

Considering first the actions between the DTCU and the B300;

P = 2 · Q = 0 (A-clock)

Refer to Figure II-12 (Page 1 of 2).

The "A" Clock pulse will occur 1μs after AQF was RESET. With this pulse character; two is placed into the "A" Register, AQF is SET, and BTDM is triggered.

DQF is not set at this time because BQF is ON. The logic to set DQF is true ON the first "A" Clock pulse only.

P = 2 Universal State

With ATDM and BTDM triggered, ITCL is sent to the B300 where it will produce one CCP. In the B300, the CCP will count MAR + 1 and will initiate a Memory Read cycle making the third character available to the DTCU.

Since AQF is now ON, the "A" Clock is disabled until AQF is RESET. Considering now the actions between the DTCU and the CTU;

When the "B" Clock pulse resets DQF at P = 2 · ITU = 1 · BQ = 1 · DQ = 1 "B" Clock, ICTL is sent to the CTU. This logic is found under the flag; P = 2 · ITU = 1 · BQ = 1 · DQ = 0 "B" Clock.

It is important to note that ICTL is a level not now dependent on the "B" Clock and that a "B" Clock pulse will not be called for until the CTU returns TCT = 1 (Terminal Character Time). This will not occur until the CTU accepts the first character. The upshot of this is that no further action will take place in the DTCU and, therefore, the B300 waits until the CTU accepts the first character.

B486 (CTU) Operation

Refer to Figure II-29.

The System Write is initiated in the CTU at Ø = 1 · P = 0 when the CTU requires System Attention (R2F); no Channels require Attention (ACANS/); the DTCU Scanner has located this CTU (TUDS); and the Central Processor and DTCU have Information available (ICTS).

Ø = 01 · P = 2

Refer to Figure II-34.

The Address of the Buffer to which the Processor will write, is transferred from the "T" to the "S" Register. Orders are SET to 07 with R = 3, indicating that the CTU is in a Write Status.

Ø = 07 · P = 1 · X = 03

On the Initial Entry to P = 1, the first character from System is in "DA" but the Memory cycle is inhibited (HMCL) because "Q" is equal zero. This action caused the first character to be discarded.

The CTU idles until the next character is available from the DTCU as indicated by ICTS. When this occurs, a Clock pulse is generated which;

1. Sets Q1F to allow counting of the "Z" Register with successive Clock pulses.
2. Transfers the TC number from the Write lines into the "DA" Register with Q = 00.
3. Initiates a Memory cycle to store the TC number in Memory.

TCTL is returned to the DTCU to indicate that the CTU is ready for the next character. Note that TCTL is sent to the DTCU as long as the CTU is at Ø = 7 · P = 1. The CTU idles until ICTS indicates that the DTCU has another character available. At this time, another Clock pulse is generated which causes the following actions to occur:

1. The "Z" Register is counted from zero to one, but proper state of the gate transfers the character into the "DB" Register (DBWS).
2. ZIF found set, writes the character from the "DB" Register into Memory (HRDBL).

The CTU idles until ICTS is returned from the DTCU to store the next

character via the "DC" Register. After the three characters are stored at the one Address, Z = 2 counts the "X" Register to address the next cell as the "Z" Register is cleared to zero.

Successive characters are stored in the same manner as just described until a Group Mark or End-Of-Memory terminates the Write. "Q" is SET to 03 at this time so that the next Clock Pulse will clear the "X" and "Z" Registers to SET "P" to 7.

The following Table defines the Information flow into the buffer as controlled by the "Z" Register.

TABLE II-1.

"Z"	INTO "D"	INTO BUFFER
0	TW to DB	From DA
1	TW to DC	From DB
2	TW to DA	From DC

Ø = 07 · P = 7

The Parity and Address cells are cleared with the Write cycle. The Output Status bit is set (DB8F) to indicate that this channel is ready to send a Reply segment to the RTU. The above action is disabled and DB4F is SET to flag System Attention for this channel when the Read/ Write Alternate switch is thrown.

Ø = 07 · P = 6

The Status bit is written into Scratchpad from the "DB" Register. DB8F is written when the channel is ready to reply to the RTU or, DB4F is written when a Test function is being performed. ØQCS sets Orders back to 01. The "P", "X" and "Z" Registers are cleared to zero and the "R" Register is set to 1 to initiate a Scan of all buffers to check if they require System Attention.

When the "R" Register is set to one, the CTU is no longer Write-Ready and the DTCU is informed of this.

DTCU Operation

As the DTCU is waiting for the CTU to come into Sync, the situation is;

1. Character number one is in the "B" Register (will be discarded by CTU).
2. Character number two is in the "A" Register (T.C. number).
3. Character number three is on the information lines from the B300.

Functional Detail

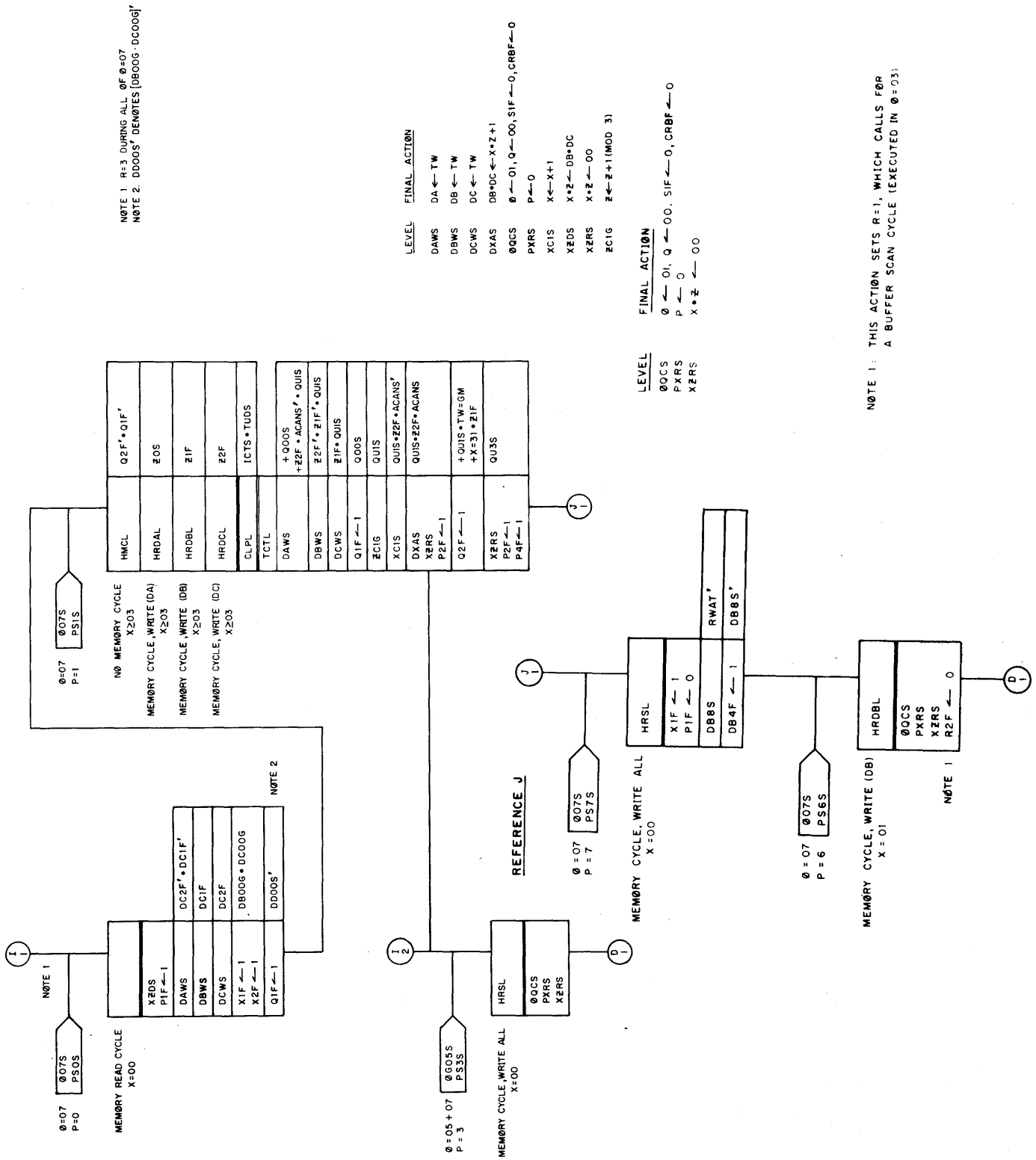


FIGURE II-34
WRITE FROM DTCU FLOW 1 & 2

P = 2 · ITU = 1 · BQ = 1 · DQ = 0 (B-clock)

Refer to Figure II-12 (Page 2 of 2).

When the CTU accepts the first character, it will send TCT = 1 (Terminal Character Time) to the DTCU causing a "B" Clock pulse. This pulse will transfer the second character into the "B" Register and will set DQF disabling ICTL to the CTU. Note that BQF will remain ON.

P = 2 · ITU = 1 · BQ = 1 · DQ = 1 (B-clock)

This "B" Clock pulse will reset AQF to enable the "A" Clock and will RESET DQF to send ICT to the CTU to enable its Clock.

P = 2 · Q = 0 (A-clock)

Refer to Figure II-12 (Page 1 of 2).

With the "A" Clock pulse, a character is placed into the "A" Register, AQF is set and BTDM is triggered.

With BTDM and ATDM both ON, the 4μs pulse ICTL is sent to the Processor requesting the next character.

Once the CTU reaches Ø = 7 · P = 1 for the information transfer, it sends TCTL to the DTCU until the transfer is complete. In the DTCU, the "B" Clock is enabled by TCTL or essentially DQ = 1. Because of this, the "B" Clock is free running and establishes the transfer rate of approximately 71 kc (14μs per character). That is, there are two "B" Clock pulses produced for each character transferred.

The "B" Clock pulse produced by TCTL places a character into the "B" Register and makes it available to the CTU. This "B" CLP also sets DQF which removes ICTL from the CTU disabling its Clock. The second "B" Clock pulse is produced by DQF and RESETS AQF and DQF. With DQF OFF, ICTL is sent to the CTU producing a Clock pulse so that it can store the character on the information lines.

With AQF ON, the "A" Clock will be enabled and will place a character into the "A" Register. The "A" Clock pulse will also trigger ATDM and BTDM. These two multis ON will send ITCL to the B300 producing one CCP to count MAR + 1 and read the next character.

GROUP MARK ENDING

B300 Operation

CUF = 3 · MC1F

Refer to Figure II-23.

After reaching the Group Mark, the Processor will hold it in the CIF until the DTCU accepts it in its "A" Register. When this occure, ITCL

is returned to the B300 for the last time proving a CCP. With this CCP, the B300 recognizes GM in the CIF and SETS RUNF and CUF to 15 completing the instruction.

B249 Operation

P = 2 · Q = 0 (A-clock)

Refer to Figure II-12 (Page 1 of 2).

The "A" Clock pulse places the Group Mark into the "A" Register and SETS AQF. BTDM is triggered to provide the B300 with the final ITCL. Since the "A" Register now contains a Group Mark (A=111111), the "A" Clock is disabled.

P = 2 · ITU = 1 · BQ = 1 · DQ = 0 (B-clock)

Refer to Figure II-12 (Page 2 of 2).

As the CTU accepts the character immediately preceeding the Group Mark, a "B" Clock pulse places the GM into the "B" Register and SETS DQF.

P = 2 · ITU = 1 · BQ = 1 · DQ = 1 (B-clock)

This "B" Clock pulse RESETS AQF and DQF as usual. In addition, "Q" is SET equal to one because the "A" Register contains a Group Mark.

Resetting AQF at this point normally enables the "A" Clock, but since the "A" Register contains a Group Mark, the "A" Clock is disabled.

P = 2 · ITU = 1 · BQ = 1 · DQ = 0 (B-clock)

Shortly after the CTU has accepted the Group Mark, the "B" Clock pulse will;

1. Reset BQF because Q $\neq$ 0.
2. Set Q to three because Q = 1.

P = 2 · Q = 3 (A-clock)

Refer to Figure II-12 (Page 1 of 2).

The "A" Clock will not be enabled until after the CTU has changed state (WR = 0).

Although the CTU has stored the Group Mark, its Clock is still dependent on the DTCU. Because of this, ICTL is generated to provide the CTU with a CCP to escape from the transfer and go back on its own Clock.

After the CTU changes its System state (WR = 0), an "A" Clock pulse is produced clearing "P" and "Q" returning the DTCU to its Idle state.

CTU Operation

Ø = 7 · P = 1

Refer to Figure II-34.

When the Group Mark is recognized on the information lines from the DTCU, (TW = GM), Q2F is SET resulting in Q = 3.

The final ICTS arriving from the DTCU produces a CCP. "Q" is now found equal three causing "P" to be SET to seven.

Ø = 7 · P = 7

DB8F is SET to store the Output status in Scratchpad.

Ø = 7 · P = 6

Order is SET to 1 and "P" is cleared while "R" is SET to 1 to initiate a Scan Cycle. It is at this point that the CTU changes state and provides the DTCU with WR = 0 so that it can return to its Idle state.

FINAL ADDRESS ENDING

CTU Operation

Ø = 7 · P = 1

As the CTU accepts the next to last character to be stored, "X" is equal to 31 and "Z" is stepped to one. Because of X = 31 · Z1F, Final Buffer Location (FBL) is sent to the DTCU to inform it that only one more character can be accepted by the CTU.

DTCU Operation

The situation at the DTCU is;

1. The final character is in the "A" Register.
2. An extra character is on the information lines from the B300 but is of no consequence. This extra character was read by the Processor because of the ITCL that was produced when the final character was placed into the "A" Register.

P = 2 · ITU = 1 · BQ = 1 · DQ = 0 (B-clock)

Refer to Figure II-12 (Page 2 of 2).

Shortly after the CTU accepts the next to last character, a "B" Clock pulse will;

1. Place the final character in the "B" Register.

2. SET DQF.
3. SET Q = 2 because FBL = 1 (Final Buffer Location).

Because "Q" is equal two, the "A" Clock is now disabled.

P = 2 · ITU = 1 · BQ = 1 · DQ = 1 (B-clock)

This "B" CLP RESETS AQF and DQF. At this point, ICTL is sent to the CTU so that it can store the Final character. Simultaneously the Processor is informed that it is no longer needed for the transfer and may therefore exit the instruction.

P = 2 · Q = 2 (A-clock)

Refer to Figure II-12 (Page 1 of 2).

The "A" Clock pulse will place the extra character into the "A" Register. Note that AQF is NOT set. More significantly as far as the B300 is concerned, is the fact that BTDM is triggered and "Q" is set to 3. Now the DTCU is sending the four microsecond Timing pulse ITCL to the B300 accompanied by IFAL (Inquiry Final Address).

B300 Operation

CUF = 3 · MC1F

Refer to Figure II-23.

A CCP is produced by ITCL. IFAL is now found true setting RUNF and CUF to 15 completing the instruction.

CTU Operation

While the DTCU is at P = 2 · Q = 2 it is sending ICTL to the CTU to hold its Clock enabled.

Ø = 7 · P = 1

Refer to Figure II-33.

When the CTU receives the Final character, X = 31 · Z1F will be found true setting Q2F (Q = 3).

Since the DTCU is keeping ICTS available, the CTU Clock will remain enabled. The next CCP will find Q = 3 (QU3S) to SET P = 7.

Ø = 7 · P = 6

From here, the CTU will return to the Idle state (Ø = 1 · P = 0) while R2F is RESET. With R2F OFF, the CTU is no longer Write-Ready and the DTCU is so informed.

DTCU Operation

P = 2 · Q = 3

Refer to Figure II-12 (Page 1 of 2).

As soon as the CTU is Not Write-Ready, WR = 0 becomes the final enabling leg on the "A" Clock. The "A" CLP will clear "P" and "Q" returning the DTCU to its Idle state.

Circuit Detail

"A" REGISTER LOAD - (NORMAL & REVERSE)

The "A" Register serves as an Input Buffer for all information sent to the DTCU. The DTCU receives the information from up to three possible external sources as follows:

1. Processing System (B300/B5500) - Sync or Write Transfer.
2. DTTU (B487) - Sync or Read Transfer.
3. Inquiry Terminal Units (B481, B483, B484 & B486) - Sync or Read Transfer.

A false level represents a 1-bit from System or Inquiry Terminal Units and a true level represents a 1-bit from DTTUs.

Because of this difference in bit representation, the "A" Register is loaded in reverse when information is received from System or Inquiry TUs, and normal when received from DTTUs.

Figure III-1 illustrates the 1-bit position of the "A" Register and associated logics. A typical example of a one (1) being received from a DTTU is as follows:

> Since a one (1) is represented by a true level from a DTTU, the Input to IN1S/ will be true causing the Output of IN1S to be true also.

The Output of AINS ("A" Register Input Normal Switch) will be true since the bit being received is not from System or Inquiry TU.

With AINS and IN1S both true, A1F is SET at A-Clock time.

A typical example of a one (1) being received from System or Inquiry TUs is as follows:

> Since a one (1) is represented by a false level from either System or Inquiry TU, the Output of IN1S/ will be true.

The Output of AIRS ("A" Register Input Reverse Switch) will also be true since the bit being received is not from a DTTU.

With AIRS and IN1S/ both true, A1F is SET at A-Clock time.

SEE PAGE 2 FOR FIGURE III-1

Circuit Detail

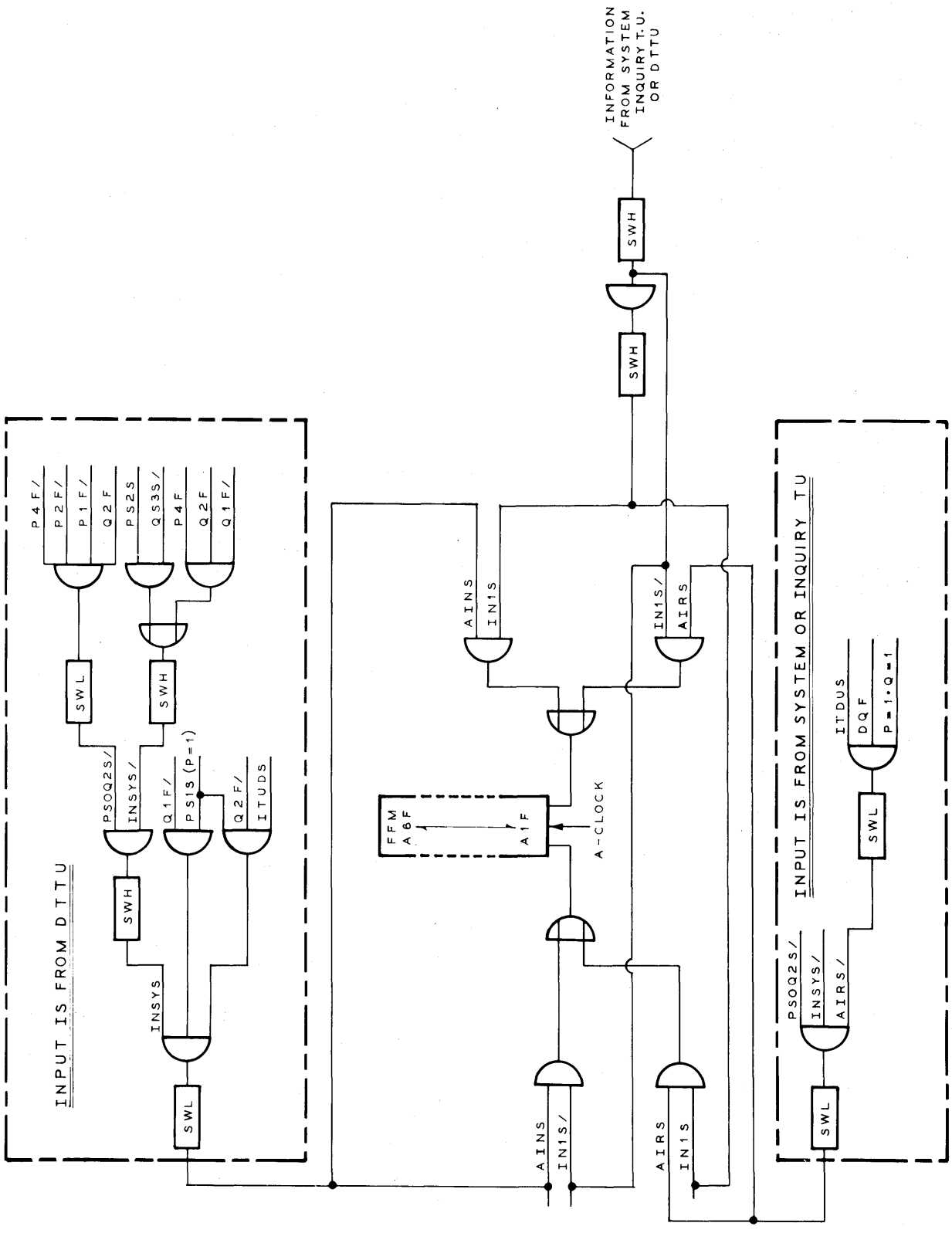


FIGURE III-1
"A" REGISTER LOAD LOGICS

Circuit Detail

SCAN

The purpose of SCAN is to locate a Terminal Unit, either DTTU or ITU, that has expressed the desire for System Attention.

The DTCU begins a progressive designation of Terminal Units (possible 15) until the one in the Interrupt State is located.

When the Terminal Unit is located, the Interrupt Flip-flop (INTF) is SET to notify the Processing System and SCAN is terminated.

P = 0 · Q = 0

Refer to Figure III-2, SCAN - Block Diagram; and Figure III-3, SCAN FLOW.

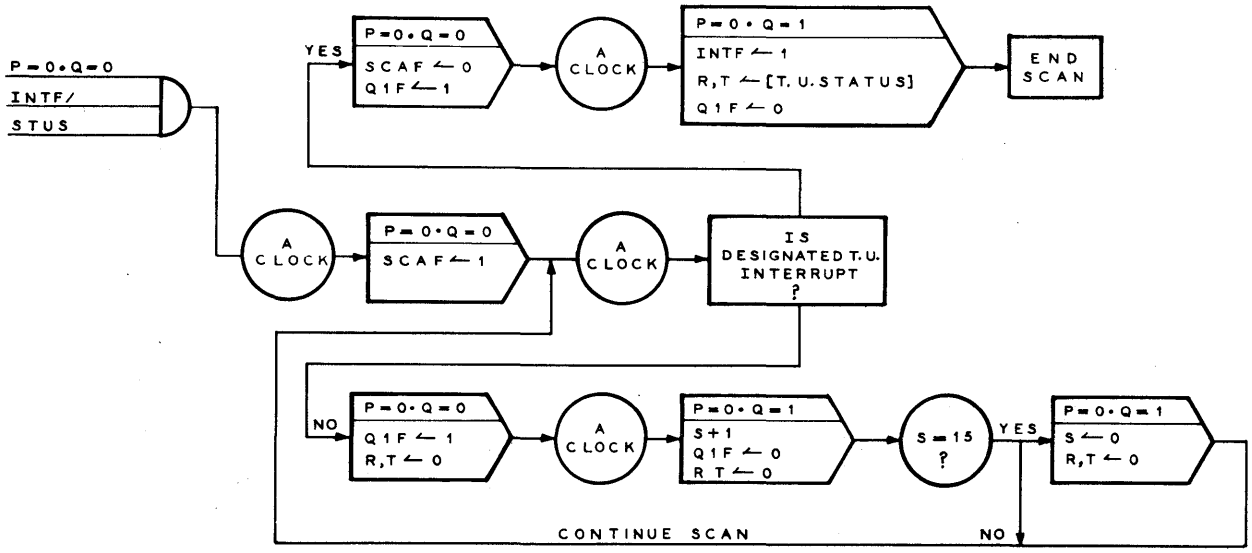


FIGURE III-2
SCAN - BLOCK DIAGRAM

Before a Scan Operation can begin, the DTCU must be Idle and the Interrupt Flip-flop OFF.

With the above conditions, any TU in an Interrupt State will generate an A-Clock and turn ON the Scan Flip-flop.

With the Scan Flip-flop ON, another A-Clock is produced which SETS Q = 1 and RESETS the "R" and "T" Registers.

P = 0 · Q = 1

Another A-Clock is generated that unconditionally RESETS Q1F.

If the Scan Flip-flop is OFF, the TU in the Interrupt State was found at P = 0 · Q = 0. SET the Interrupt Flip-flop and terminate SCAN. If

Circuit Detail

the Terminal Unit is of the Inquiry type, load the "R" and "T" Registers with the TU status.

If the Scan Flip-flop (SCAF) is ON, the TU in the Interrupt State was not found at P = 0 · Q = 0. Count S plus 1 if S ≠ 15, or, RESET S if S = 15. Clear the "R" and "T" Registers and return to P = 0 · Q = 0 with SCAF ON and continue SEARCH.

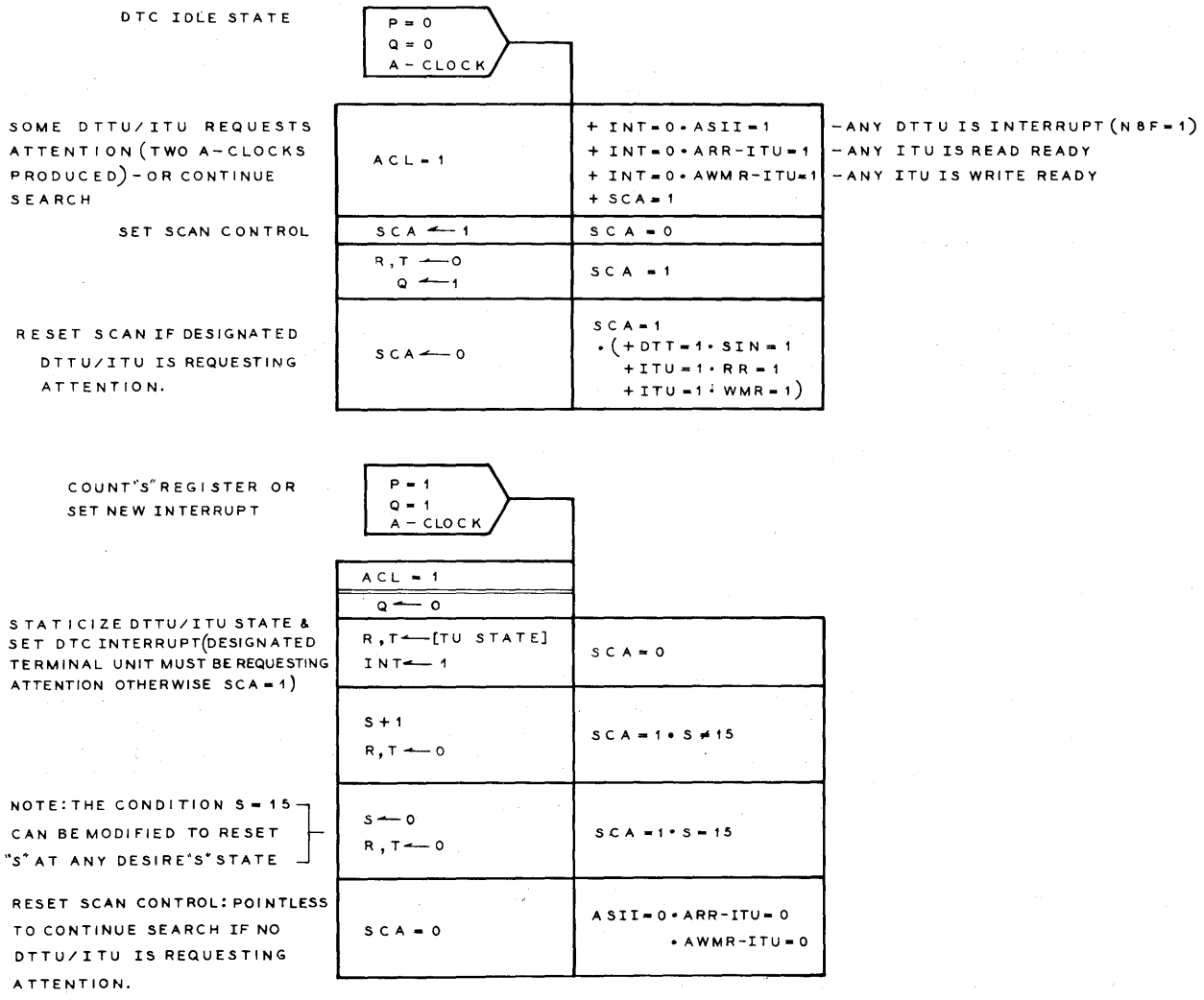


FIGURE III-3
SCAN FLOW

TRANSLATOR

A two-way translation of the ASCII and Baudot Character Code Set is provided in the B249 DTCU. Information transferred to the System is converted to Burroughs Common Language Code (BCL). A BCL to Baudot translation takes place when information is being sent to a Teletype Adapter (981) or Terminal Unit (B481). A BCL to ASCII translation takes place when the System sends information to an Adapter or Inquiry

Circuit Detail

Terminal operating in ASCII code. Adapters operating in BCL code require no translation. Therefore, the Decoding and Encoding circuits of the Translator are by-passed.

The routing of information through the Translator is shown in Figure III-4.

All data to be translated, whether going to or from the System, will be SET into the "A" Register. The Output of the "A" Register is divided into two groups: Zone (B, A & 8) and Numeric (4, 2 & 1). The three Zone and three Numeric bits are gated to the "A" Register Decoder to produce 8 Zone levels (AZnG) and 8 Numeric levels (ANnG).

The Zone and Numeric levels from the "A" Register Decoder will enable one of the 64 Character Decoder gates which in turn will enable the Character Switch that carries the Octal designation of the Input Character. The Character Switch Output will then enable the Encoding circuits. The type of operation being performed (System Read or Write) and the state of the "T" Register (Translation Selection Circuit) will select the proper Encoder Selection Switch for the type of translation desired. The Encoder Output Switches are SET into the "B" Register and then sent to the System or designated Terminal Unit.

TRANSLATION SELECTION

The Translation Selection Circuit consists of a two-bit Translation Register and its associated Input gating. The setting of this Register is controlled by the designated Adapter and/or Terminal Unit which will result in one of the following states:

1. T = 0 - The Designated Terminal or Adapter is operating in Baudot code.

2. T = 1 - The Designated Terminal or Adapter is operating in ASCII code.

3. T = 2 - The Designated Adapter does not require translation.

When the designated Terminal is a Typewriter (B483), Dial TWX (B484) or Central (B486), the level TUR1L/ from the TU will be false and SET the "T" Register equal to one.

If the System is performing a Read operation, an ASCII to BCL translation is performed. A Write operation results in a BCL to ASCII translation.

If the designated TU is a Teletype (B481), TUR1L/ is true, the "T" Register is cleared and a Baudot to BCL to Baudot translation takes place.

When the designated Terminal is a DTTU (B487), the "T" Register setting for the type Adapter designated is shown in Table III-1.

Circuit Detail

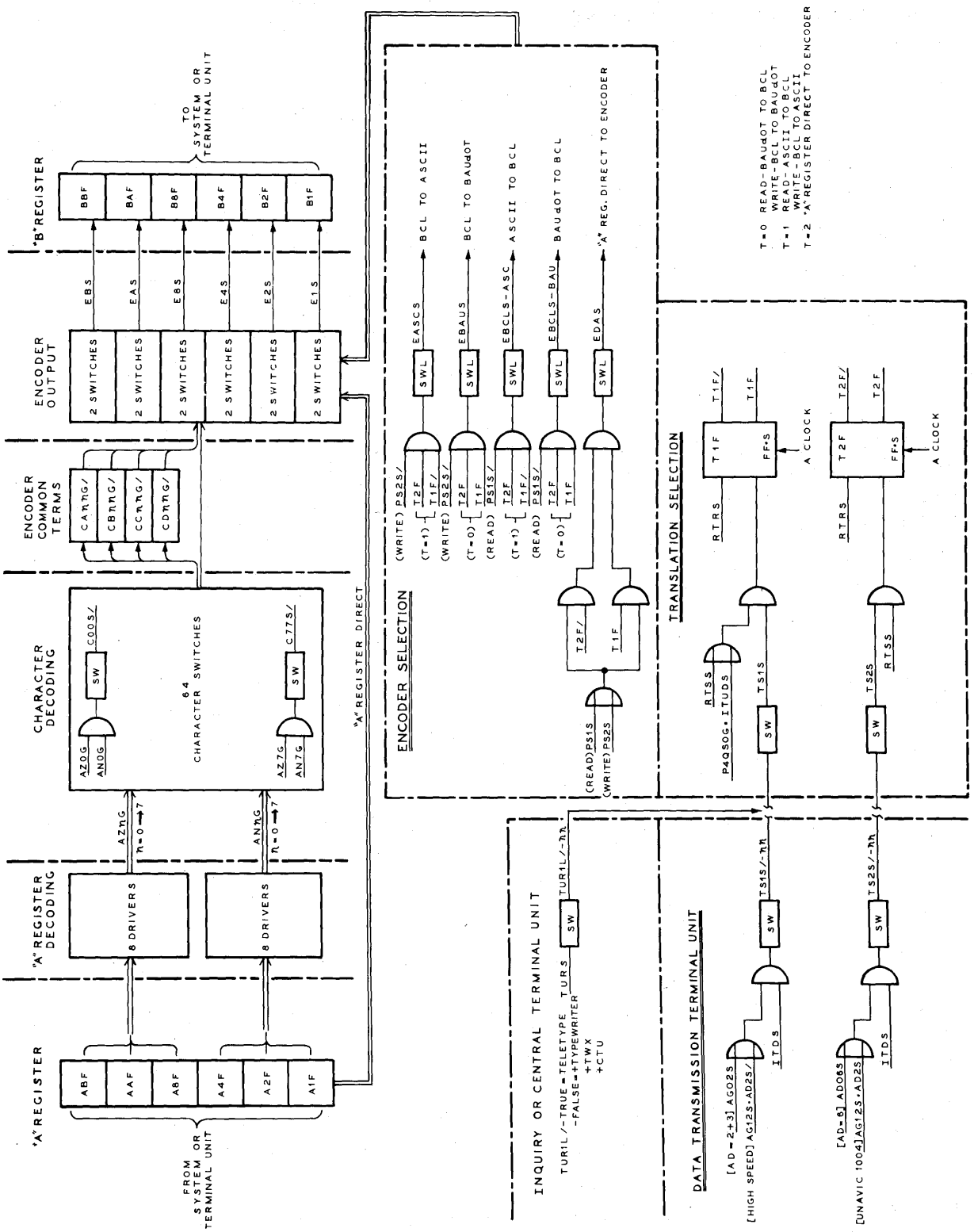


FIGURE III-4
TRANSLATOR - LOGICS

Circuit Detail

TABLE III-1. TRANSLATION SELECTION

ADAPTER DESIGNATION	ADAPTER	ADAPTER CODE	"T" REGISTER
AD = 1	TELETYPE (981)	BAUDOT	0
AD = 2	DATASPEED (982)	10 UNIT ASCII	1
AD = 3	TWX/TYP (980)	11 UNIT ASCII	1
AD = 4	UNASSIGNED		-
AD = 5	UNASSIGNED		-
AD = 6	IBM 1050 (985) , ACU (983)	PTT/6 , BCL-NUMERIC	2
AD = 7	UNASSIGNED		-
AD = 8	UNASSIGNED		-
AD = 9	UNASSIGNED		-
AD = 10	UNASSIGNED		-
AD = 11	UNASSIGNED		-
AD = 12	HIGH SPEED (HONEYWELL H120)	ASCII	1
AD = 13	UNASSIGNED		-
AD = 14	UNIVAC 1004 (984)	BCL	2
AD = 15	UNASSIGNED		-

ENCODER SELECTION

The Encoder Selection circuit will determine the type of translation performed by controlling the Input gating of the Encoder Output Switches.

This circuit consists of the following five switches and their associated Input gates:

1. EASCS - Encode ASCII from BCL

   True during System Write operations with the "T" Register equal to one (1).

2. EBAUS - Encode Baudot from BCL

   True during System Write operations with the "T" Register equal to zero (0).

3. EBCLS-ASC - Encode BCL from ASCII

   True during System Read operations with the "T" Register equal to one (1).

4. EBCLS-BAU - Encode BCL from Baudot

   True during System Read operations with the "T" Register equal to zero (0).

5. EDAS - Encode Direct from"A" Register

   True during System Read or Write operations when the "T" Register is equal to two (2). When this condition exists, the contents of the "A" Register will be gated directly into the Encoder Output Switches and then into the "B" Register. No translation is performed.

OCTAL NUMBERING SYSTEMS

The Octal Numbering System works to a base 8. All data is represented with the numbers 0 thru 7. If a number larger than seven is required, the next column receives a Carry while the present column adjusts to produce the Octal weight required. For example: Decimal 8 = Octal 10, Decimal 9 = Octal 11, Decimal 63 = Octal 77 etc.

The Octal designation of the character determines which one of the 64 Character switches in the Translator is enabled. The Octal value of the codes is determined in the following manner:

1. The Zone bits (B, A, 8) are assigned the binary weights of 4, 2 and 1.

2. The Numeric bits (4, 2, 1) are assigned the binary weights of 4, 2 and 1.

The actual value of a character is determined by reading the binary equivalent of the Zone bits (B, A, 8) and of the Numeric bits (4, 2, 1) as shown below.

CODE	ZONE	NUMERIC	OCTAL VALUE
BCL Z	011	001	31
BAUDOT Z	010	001	21
BCL K	100	010	42
BAUDOT /	111	101	75

INPUT LOGICS

The primary function of the "A" Register Decoding circuit is to determine the Octal value of the character being decoded. All codes that have the same Octal value will enable the same circuits as shown below.

OCTAL VALUE	BCL CODE	ASCII CODE	BAUDOT CODE	BINARY REPRESENTATION
11	9	I	D	001001
36	]	↑	V	011110
76	<	>	;	111110

This means that a D from a TTY Adapter will enable the same circuits as an I from a TWX/TYP Adapter or a 9 from the System.

The Zone and Numeric Octal values are gated together to produce one level that represents the combined Octal value of the character. This level is fed into one of the 64 Character Switches in the Translator.

Refer to Tables III-2 and III-3. They show the translation from one code to another along with the Character Switch that is enabled for each code.

Circuit Detail

TABLE III-2

"A" REGISTER ASCII	BA 8421	CHARACTER SWITCH	"B" REGISTER BCL	BA 8421
SPACE	10 0000	C40S/	BLANK	01 0000
•	10 1110	C56S/	•	11 1011
[	01 1011	C33S/	[	11 1100
<	10 1000	C50S/	<	11 1101
≤	11 1100	C74S/	≤	11 1110
←	01 1111	C37S/	←	11 1111
&	10 0110	C46S/	&	11 0000
$	10 0100	C44S/	$	10 1011
*	10 1010	C52S/	*	10 1100
)	10 1001	C51S/	)	10 1101
;	11 1011	C73S/	;	10 1110
!	10 0111	C47S/	!	10 1111
-	10 1101	C55S/	-	10 0000
/	10 1111	C57S/	/	01 0001
,	10 1100	C54S/	,	01 1011
%	10 0101	C45S/	%	01 1100
=	11 1101	C75S/	=	01 1101
]	01 1101	C35S/	]	01 1110
"	10 0010	C42S/	"	01 1111
#	10 0011	C43S/	#	00 1011
@	00 0000	C00S/	@	00 1100
:	11 1010	C72S/	:	00 1101
>	11 1110	C76S/	>	00 1110
!	10 0001	C41S/	!	00 1111
+	10 1011	C53S/	+	11 1010
A	00 0001	C01S/	A	11 0001
B	00 0010	C02S/	B	11 0010
C	00 0011	C03S/	C	11 0011
D	00 0100	C04S/	D	11 0100
E	00 0101	C05S/	E	11 0101
F	00 0110	C06S/	F	11 0110
G	00 0111	C07S/	G	11 0111
H	00 1000	C10S/	H	11 1000
I	00 1001	C11S/	I	11 1001
\	01 1100	C34S/	x	10 1010
J	00 1010	C12S/	J	10 0001
K	00 1011	C13S/	K	10 0010
L	00 1100	C14S/	L	10 0011
M	00 1101	C15S/	M	10 0100
N	00 1110	C16S/	N	10 0101
O	00 1111	C17S/	O	10 0110
P	01 0000	C20S/	P	10 0111
Q	01 0001	C21S/	Q	10 1000
R	01 0010	C22S/	R	10 1001
↑	01 1110	C36S/	≠	01 1010
S	01 0011	C23S/	S	01 0010
T	01 0100	C24S/	T	01 0011
U	01 0101	C25S/	U	01 0100
V	01 0110	C26S/	V	01 0101
W	01 0111	C27S/	W	01 0110
X	01 1000	C30S/	X	01 0111
Y	01 1001	C31S/	Y	01 1000
Z	01 1010	C32S/	Z	01 1001
0	11 0000	C60S/	0	00 1010
1	11 0001	C61S/	1	00 0001
2	11 0010	C62S/	2	00 0010
3	11 0011	C63S/	3	00 0011
4	11 0100	C64S/	4	00 0100
5	11 0101	C65S/	5	00 0101
6	11 0110	C66S/	6	00 0110
7	11 0111	C67S/	7	00 0111
8	11 1000	C70S/	8	00 1000
9	11 1001	C71S/	9	00 1001
?	11 1111	C77S/	?	00 0000

"A" REGISTER BCL	BA 8421	CHARACTER SWITCH	"B" REGISTER ASCII	BA 8421
BLANK	01 0000	C20S/	SPACE	10 0000
•	11 1011	C73S/	•	10 1110
[	11 1100	C74S/	[	01 1011
<	11 1101	C75S/	<	10 1000
≤	11 1110	C76S/	≤	11 1100
←	11 1111	C77S/	←	01 1111
&	11 0000	C60S/	&	10 0110
$	10 1011	C53S/	$	10 0100
*	10 1100	C54S/	*	10 1010
)	10 1101	C55S/	)	10 1001
;	10 1110	C56S/	;	11 1011
!	10 1111	C57S/	!	10 0111
-	10 0000	C40S/	-	10 1101
/	01 0001	C21S/	/	10 1111
,	01 1011	C33S/	,	10 1100
%	01 1100	C34S/	%	10 0101
=	01 1101	C35S/	=	11 1101
]	01 1110	C36S/	]	01 1101
"	01 1111	C37S/	"	10 0010
#	00 1011	C13S/	#	10 0011
@	00 1100	C14S/	@	00 0000
:	00 1101	C15S/	:	11 1010
>	00 1110	C16S/	>	11 1110
!	00 1111	C17S/	!	10 0001
+	11 1010	C72S/	+	10 1011
A	11 0001	C61S/	A	00 0001
B	11 0010	C62S/	B	00 0010
C	11 0011	C63S/	C	00 0011
D	11 0100	C64S/	D	00 0100
E	11 0101	C65S/	E	00 0101
F	11 0110	C66S/	F	00 0110
G	11 0111	C67S/	G	00 0111
H	11 1000	C70S/	H	00 1000
I	11 1001	C71S/	I	00 1001
x	10 1010	C52S/	\	01 1100
J	10 0001	C41S/	J	00 1010
K	10 0010	C42S/	K	00 1011
L	10 0011	C43S/	L	00 1100
M	10 0100	C44S/	M	00 1101
N	10 0101	C45S/	N	00 1110
O	10 0110	C46S/	O	00 1111
P	10 0111	C47S/	P	01 0000
Q	10 1000	C50S/	Q	01 0001
R	10 1001	C51S/	R	01 0010
≠	01 1010	C32S/	↑	01 1110
S	01 0010	C22S/	S	01 0011
T	01 0011	C23S/	T	01 0100
U	01 0100	C24S/	U	01 0101
V	01 0101	C25S/	V	01 0110
W	01 0110	C26S/	W	01 0111
X	01 0111	C27S/	X	01 1000
Y	01 1000	C30S/	Y	01 1001
Z	01 1001	C31S/	Z	01 1010
0	00 1010	C12S/	0	11 0000
1	00 0001	C01S/	1	11 0001
2	00 0010	C02S/	2	11 0010
3	00 0011	C03S/	3	11 0011
4	00 0100	C04S/	4	11 0100
5	00 0101	C05S/	5	11 0101
6	00 0110	C06S/	6	11 0110
7	00 0111	C07S/	7	11 0111
8	00 1000	C10S/	8	11 1000
9	00 1001	C11S/	9	11 1001
?	00 0000	C00S/	?	11 1111

Circuit Detail

TABLE III-3

"A" REGISTER BCL	BA	8421	CHARACTER SWITCH	"B" REGISTER BAUDOT	A	8421
BLANK	01	0000	C20S/	SPACE	00	0100
•	11	1011	C73S/	•	11	1100
[	11	1100	C74S/	FIGS	11	1011
(	11	1101	C75S/	(	10	1111
<	11	1110				
←	11	1111	C77S/	BLANK	00	0000
&	11	0000	C60S/	&	11	1010
$	10	1011	C53S/	$	10	1001
*	10	1100	C54S/	*	10	1011
)	10	1101	C55S/	)	11	0010
;	10	1110	C56S/	;	11	1110
≤	10	1111	C57S/	CR	00	1000
-	10	0000	C40S/	-	10	0011
/	01	0001	C21S/	/	11	1101
,	01	1011	C33S/	,	10	1100
%	01	1100				
=	01	1101				
]	01	1110	C36S/	LTRS	01	1111
"	01	1111	C37S/	"	11	0001
#	00	1011	C13S/	DISCONN	11	0100
@	00	1100				
:	00	1101	C15S/	:	10	1110
>	00	1110				
≥	00	1111	C17S/	!	10	1101
+	11	1010				
A	11	0001	C61S/	A	00	0011
B	11	0010	C62S/	B	01	1001
C	11	0011	C63S/	C	00	1110
D	11	0100	C64S/	D	00	1001
E	11	0101	C65S/	E	00	0001
F	11	0110	C66S/	F	00	1101
G	11	0111	C67S/	G	01	1010
H	11	1000	C70S/	H	01	0100
I	11	1001	C71S/	I	00	0110
X	10	1010	C52S/	BELL	10	0101
J	10	0001	C41S/	J	00	1011
K	10	0010	C42S/	K	00	1111
L	10	0011	C43S/	L	01	0010
M	10	0100	C44S/	M	01	1100
N	10	0101	C45S/	N	00	1100
O	10	0110	C46S/	O	01	1000
P	10	0111	C47S/	P	01	0110
Q	10	1000	C50S/	Q	01	0111
R	10	1001	C51S/	R	00	1010
≠	01	1010	C32S/	LF	00	0010
S	01	0010	C22S/	S	00	0101
T	01	0011	C23S/	T	01	0000
U	01	0100	C24S/	U	00	0111
V	01	0101	C25S/	V	01	1110
W	01	0110	C26S/	W	01	0011
X	01	0111	C27S/	X	01	1101
Y	01	1000	C30S/	Y	01	0101
Z	01	1001	C31S/	Z	01	0001
0	00	1010	C12S/	0	11	0110
1	00	0001	C01S/	1	11	0111
2	00	0010	C02S/	2	11	0011
3	00	0011	C03S/	3	10	0001
4	00	0100	C04S/	4	10	1010
5	00	0101	C05S/	5	11	0000
6	00	0110	C06S/	6	11	0101
7	00	0111	C07S/	7	10	0111
8	00	1000	C10S/	8	10	0110
9	00	1001	C11S/	9	11	1000
?	00	0000	C00S/	?	11	1001

"A" REGISTER BAUDOT	BA	8421	CHARACTER SWITCH	"B" REGISTER BCL	BA	8421
SPACE	00	0100	C04S/	BLANK	01	0000
•	11	1100	C74S/	•	11	1011
FIGS	11	1011	C73S/	[	11	1100
(	10	1111	C57S/	(	11	1101
BLANK	00	0000	C00S/	←	11	1111
&	11	1010	C72S/	&	11	0000
$	10	1001	C51S/	$	10	1011
*	10	1011	C53S/	*	10	1100
)	11	0010	C62S/	)	10	1101
;	11	1110	C76S/	;	10	1110
CR	00	1000	C10S/	≤	10	1111
-	10	0011	C43S/	-	10	0000
/	11	1101	C75S/	/	01	0001
,	10	1100	C54S/	,	01	1011
LTRS	01	1111	C37S/	]	01	1110
"	11	0001	C61S/	"	01	1111
DISCONN	11	0100	C64S/	#	00	1011
:	10	1110	C56S/	:	00	1101
!	10	1101	C55S/	≥	00	1111
A	00	0011	C03S/	A	11	0001
B	01	1001	C31S/	B	11	0010
C	00	1110	C16S/	C	11	0011
D	00	1001	C11S/	D	11	0100
E	00	0001	C01S/	E	11	0101
F	00	1101	C15S/	F	11	0110
G	01	1010	C32S/	G	11	0111
H	01	0100	C24S/	H	11	1000
I	00	0110	C06S/	I	11	1001
BELL	10	0101	C45S/	X	10	1010
J	00	1011	C13S/	J	10	0001
K	00	1111	C17S/	K	10	0010
L	01	0010	C22S/	L	10	0011
M	01	1100	C34S/	M	10	0100
N	00	1100	C14S/	N	10	0101
O	01	1000	C30S/	O	10	0110
P	01	0110	C26S/	P	10	0111
Q	01	0111	C27S/	Q	10	1000
R	00	1010	C12S/	R	10	1001
LF	00	0010	C02S/	≠	01	1010
S	00	0101	C05S/	S	01	0010
T	01	0000	C20S/	T	01	0011
U	00	0111	C07S/	U	01	0100
V	01	1110	C36S/	V	01	0101
W	01	0011	C23S/	W	01	0110
X	01	1101	C35S/	X	01	0111
Y	01	0101	C25S/	Y	01	1000
Z	01	0001	C21S/	Z	01	1001
0	11	0110	C66S/	0	00	1010
1	11	0111	C67S/	1	00	0001
2	11	0011	C63S/	2	00	0010
3	10	0001	C41S/	3	00	0011
4	10	1010	C52S/	4	00	0100
5	11	0000	C60S/	5	00	0101
6	11	0101	C65S/	6	00	0110
7	10	0111	C47S/	7	00	0111
8	10	0110	C46S/	8	00	1000
9	11	1000	C70S/	9	00	1001
?	11	1001	C71S/	?	00	0000

Circuit Detail

The Character Switch name represents the Octal value of the code being translated. The result of the translation is shown in the columns headed BCL to ASCII, BCL to Baudot, ASCII to BCL and Baudot to BCL.

For example:

The BCL], or the ASCII ↑, or the Baudot V all have an Octal value of 36. During a BCL to ASCII translation of a], Character Switch 36 will produce the ASCII code for this character (011101). During a BCL to Baudot translation of the], the Baudot letters code (011111) is produced. When a Baudot V is translated through Switch 36, a BCL V (010101) is produced.

The Character Switch Outputs feed the Encoder gates, and to conserve diodes, the Character Switches also feed common AND gates whenever feasible.

CHARACTER SWITCH	BCL TO X3.2	BCL TO BAUDOT	BAUDOT TO BCL
	654321	*54321	BA8421
25	V 010110	V 011110	Y 011000
47	P 010000	P 010110	7 000111
50	Q 010001	Q 010111	SPACE 010000
64	D 000100	D 001001	# 001011
66	F 000110	F 001101	0 001010
67	G 000111	G 011010	1 000001

The common AND gate CA09G is one of the terms used in translating BCL to ASCII, BCL to Baudot and Baudot to BCL. It provides no function when the translation is from ASCII to BCL. The above insert shows six characters represented by CA09G when the Input is BCL (V, P, Q, D, F, G) and when it is Baudot (Y, 7, SPACE, #, 0, 1).

NOTE

The ASCII codes for the 6 character represented by CA09G are common in that the 8 and B bit positions are zero (0) in each case. Whenever one of these 6 character Switches is turned ON, EBS/ and E8S/ will go true to insert zeros in the B and 8 bit positions of the "B" Register. Similarly, CA09G will bring EBS/ true since this bit position is a zero for all 6 characters when the translation is Baudot to BCL.

CLOCK CONTROL

The DTCU utilizes two CLNQ packages to produce individual Clock Pulses labeled A-Clock and B-Clock. Both Clock Outputs are negative pulses of .5μs duration. A false Input of more than 1μs is required to produce a pulse Output.

Circuit Detail

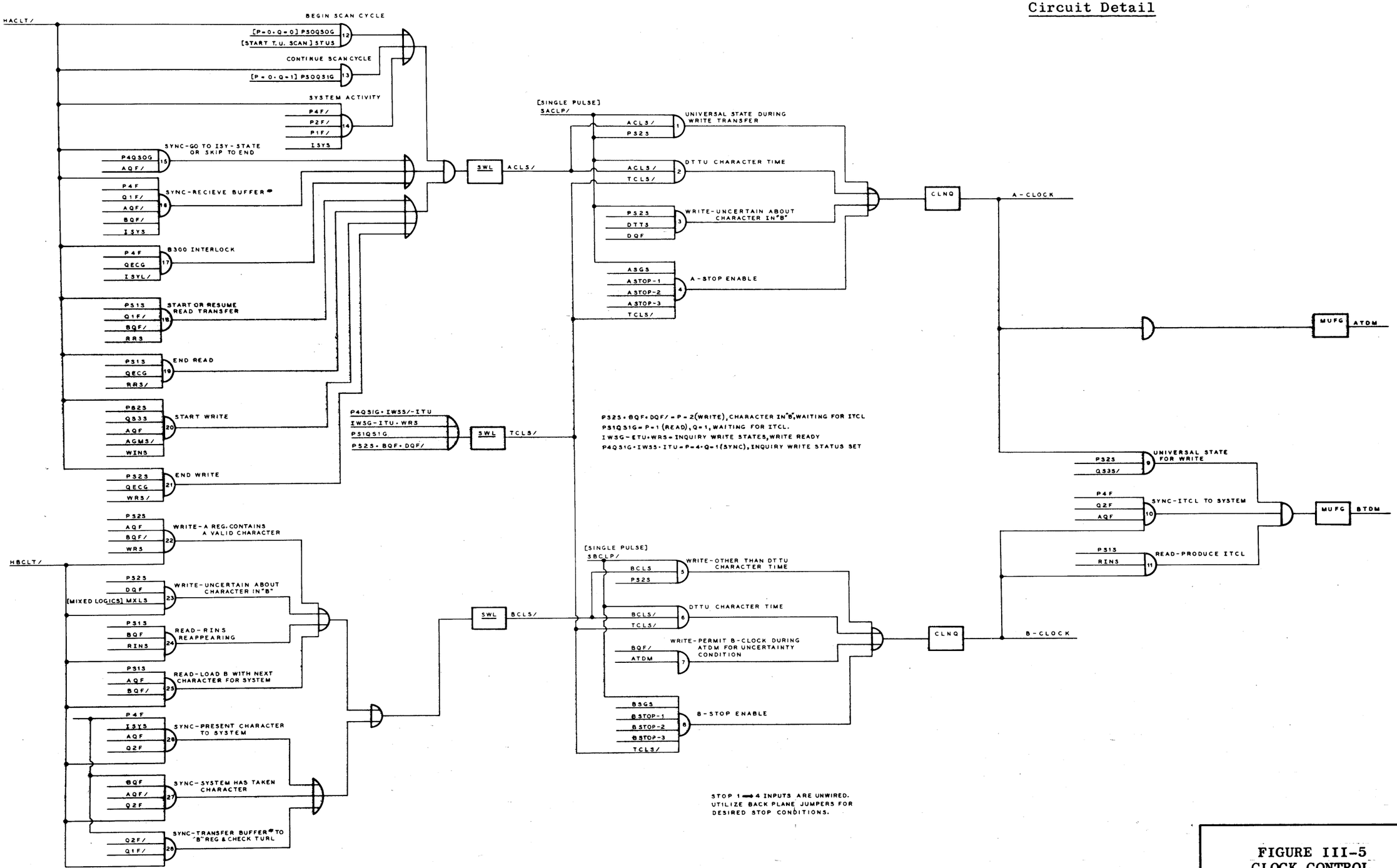


FIGURE III-5
CLOCK CONTROL

Circuit Detail

Each CLNQ has an associated Multi labeled ATDM (A-Time Delay Multi) and BTDM (B-Time Delay Multi). The purpose of ATDM and BTDM is to prevent A-Clocks and B-Clocks from occuring closer than 7 or 8μs apart to allow sufficient time for translation.

A Schematic Diagram of A-Clock, B-Clock Control with associated logics is shown in Figure III-5.

The Inputs to both CLNQs are controlled by four-legged OR gates. Since a CLNQ requires a false Input to produce an Output pulse, any one of these Inputs going true will inhibit Clock Outputs.

The Inhibit A and B Clock Toggle Switches (HACLT/ and HBCLT/) are a prime control on ACLS/ and BCLS/. With the Inhibit Clock Switch ON, HACLT/ and HBCLT/ are false and a Clock pulse can only be produced by depressing the Single Pulse button (SACLP/ or SBCLP/).

GATE 1 - Universal State During Write Transfer

Permits A-Clock during Write Transfer (PS2S) under control of ACLS/.

GATE 2 - DTTU Character Time

Permits A-Clock when the DTTU responds with a 4μs Character Time Level (TCTL).

GATE 3 - Write: Uncertain About Character in "B" Register

Inhibits A-Clock for one Clock period. This condition could occur if WIRL (from System) reappears at a unique point in time causing A and B Clocks to occur something less than 7 or 8μs apart. DQF flags this condition and A-Clock is inhibited to provide sufficient time for Character Translation.

GATE 4 - A-Stop Enable

Permits A-Clock Control with the use of the A-Clock Stop Gate Maintenance Switch and up to three Optional Conditions.

GATE 5 - Write: Other Than DTTU Character Time

Generates B-Clocks other than those produced as a result of DTTU Character Time TCLS/.

GATE 6 - DTTU Character Time

Permits B-Clock when the DTTU responds with a 4μs Character Time Level (TCTL).

GATE 7 - Permit B-Clock During ATDM For Uncertainty Condition

Insures a B-Clock even though ATDM is still true if uncertain that sufficient time was allotted for translation of the Character in the "B" Register.

GATE 8 - B-Stop Enable

Permits B-Clock Control with the use of the B-Clock Stop Gate

Maintenance Switch and up to three Optional Conditions.

GATE 9 - Universal State For Write

Permits BTDM to be fired with A-Clock during Write Transfer.

GATE 10 - SYNC: ITCL To System

Produces Inquiry Time for Character Level (ITCL) to the System during SYNC Time.

GATE 11 - Read: Produce ITCL

Produces ITCL during Read Transfer Time at a B-Clock rate. Note that should the System drop RINS, ITCL is not generated and the DTC waits for RINS to appear.

GATE 12 - Begin Scan Cycle

Produces an A-Clock to initiate a Scan Cycle when some DTTU becomes Interrupted and the DTCU in IDLE $P = 0 \cdot Q = 0$.

GATE 13 - Continue Scan Cycle

Produces A-Clocks until the Interrupt DTTU is found or the maximum "S" Register count is reached.

GATE 14 - System Activity

System activity to begin either Interrogate Read or Write. Two A-Clocks are generated with this gate. The second A-Clock will load the "S" Register with the DTTU number.

GATE 15 - SYNC: Go To ISY-STATE or Skip To End

DTCU has returned DTTU number to System and will proceed with Interrogate Read or Write provided the DTTU is Ready.

GATE 16 - SYNC: Receive Buffer Number

DTCU receives the Buffer number to be sent to the appropriate DTTU.

GATE 17 - B300 Interlock

Sync Cycle is over. Generate an A-Clock to clear the DTCU.

GATE 18 - Start Read

The DTTU is Read-Ready, produces an A-Clock to either start the Read Transfer (1st Character) or resume Read Transfer after an Interruption.

GATE 19 - End Read

Read Transfer is complete. Group Mark or BFL encountered.

GATE 20 - Start Write

The 1st Character from the System is contained in the "A" Register and WINS is present.

Circuit Detail

GATE 21 - End Write

Write Transfer is complete. Group Mark encountered.

GATE 22 - Write: "A" Register contains A Valid Character

The System has transferred a character to the "A" Register. Generate a B-Clock to transfer this character to the "B" Register and wait for the DTTU to respond.

GATE 23 - Write: Uncertain About Character In "B" Register

The condition described under GATE 3 has occurred. Generate a B-Clock to provide the necessary delay for translation.

GATE 24 - Read: RINS Reappearing

The System has dropped RINS (B5500 Memory Cycle) and is now ready to resume the Read Transfer.

GATE 25 - Read: Load "B" Register with Next Character For System

The System has taken the last character (BQF/) and the "A" Register has been filled by the DTTU. Generate a B-Clock and load the "B" Register again.

GATE 26 - SYNC: Load "B" Register With Character For System

This gate is used to return both the DTTU number and the Buffer number to the System.

GATE 27 - SYNC: System Has DTTU Number

The DTCU is assured that the System has taken the characters presented with GATE 26.

GATE 28 - SYNC: Transfer Buffer Number To "B" Register & Check TURL

The DTCU has the DTTU number in the "S" Register and the Buffer number in the "B" Register. Generate a B-Clock and, if the DTTU is Ready (TURL), SET BQF.

Adjustments

CLOCK ADJUSTMENTS

CLNQ-A

Set the Display Panel Switches as follows:

LOCAL/REMOTE Switch - LOCAL

Place all other Maintenance Switches in the OFF position.

Set the scope as follows:

Time Base - 1μs/cm
Vertical - 0.2 V/cm
Trigger - Internal - Negative

Ground the Input of CLNQ-A at pin AA C7 J1. Monitor the CLNQ-A Output at AB A1 X9; the pulse width should be 500 ns ±10%. Adjust CLNQ-A (AA C7 A2) for 7μs between pulses.

CLNQ-B

Set the Display Panel Switches as follows:

LOCAL/REMOTE Switch - LOCAL

Place all other Maintenance Switches in the OFF position.

Set the scope as follows:

Time Base - 1μs/cm
Vertical - 0.2 V/cm
Trigger - Internal - Negative

Ground the Input of CLNQ-B at pin AA C7 W1. Monitor the CLNQ-B Output at AA A9 X6; the pulse width should be 500ns ±10%. Adjust CLNQ-B (AA C7 N2) for 7μs between pulses.

VARIABLE BIAS ADJUSTMENT

The Variable Bias Package is located at AA C8 A2. Measure the bias level at AB A1 X9. Adjust the potentiometer to obtain 0.5V at this point.

Maintenance Procedures

MAINTENANCE PANEL

Figure V-1 illustrates the Maintenance Panel of the DTCU. All Toggle Switches are 3-position with the center position OFF unless otherwise specified.

The Neon Indicators are grouped under four (4) major divisions labeled SELECT, TERMINAL UNIT STATUS, CONTROL and INFORMATION.

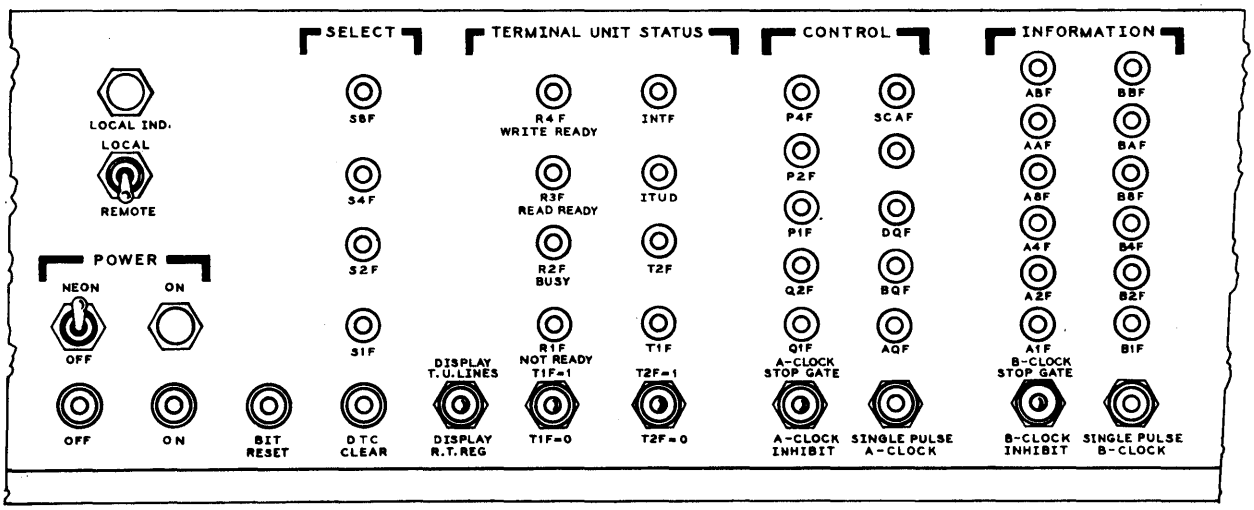


FIGURE V-1
MAINTENANCE PANEL

SELECT NEONS

The "S" Register is used to designate one out of a possible 15 Terminal Units

TERMINAL UNIT STATUS NEONS

The "R" Register is used as temporary storage for the status of a designated Buffer.

The "T" Register is used to indicate the type of translation required for a designated Buffer or ITU.

ITUD (Inquiry Unit Designate) when ON, indicates that an Inquiry Terminal Unit is designated.

INTF (Interrupt Flip-flop) is used to signal the Processing System that an Interrupt Condition exists.

CONTROL NEONS

The "P" Register is Primary Control and denotes the type of operation being performed: Interrogate, Read, Write or Scan.

AQF - When ON, indicates that the "A" Register contains pertinent information.

BQF - When ON, indicates that the "B" Register contains pertinent information.

DQF - Used to delay A-Clock for one period to provide sufficient translation time.

SCAF (Scan Flip-flop) - When ON, indicates that a Scan Cycle is in progress to locate a DTTU/ITU that has an Interrupt.

INFORMATION NEONS

The "A" Register serves as an Input Register for information coming from System or DTTU/ITU to the DTCU.

The "B" Register serves as an Output Register for information going to System or DTTU/ITU from the DTCU.

POWER ON PUSHBUTTON

When depressed, initiates a Power Up Sequence in the B452 provided the LOCAL/REMOTE Switch is in LOCAL. Any DTTU/ITU that is in REMOTE will also have power supplied.

POWER OFF PUSHBUTTON

When depressed, initiates a Power Down Sequence in the B452 provided the LOCAL/REMOTE Switch is in LOCAL. Any DTTU/ITU that is in REMOTE will also have power removed.

BIT RESET BUTTON

When depressed, causes all Neon Switch Indicators to act as Flip-flop Reset Switches instead of Flip-flop Set Switches.

DTC CLEAR

When depressed, RESETS all DTC Flip-flops.

DISPLAY TU LINES/R.T. REG.

When in the Display TU Lines position, reflects the status of the Input levels from the DTTU/ITU to the "R" and "T" Registers.

When in the Display R.T. Register position, displays the states of the "R" and "T" Register Flip-flops.

T1F = 1 + 0 · T2F = 1 + 0

Permits manual selection of translation desired by altering the value of the "T" Register setting.

A-CLOCK STOP GATE/INHIBIT

When in the A-Clock Stop Gate position, permits the A-Clock to be inhibited with up to three (3) Optional Conditions (Backplane Jumpers).

When in the A-Clock Inhibit position, permits A-Clocks to be produced with the Single Pulse A-Clock pushbutton.

SINGLE PULSE A-CLOCK

When depressed, produces an A-Clock provided the A-Clock Inhibit Switch is ON.

B-CLOCK STOP GATE/INHIBIT

When in the B-Clock Stop Gate position, permits the B-Clock to be inhibited with up to three (3) Optional Conditions (Backplane Jumpers).

When in the B-Clock Inhibit position, permits B-Clocks to be produced with the Single Pulse B-Clock pushbutton.

SINGLE PULSE B-CLOCK

When depressed, produces a B-Clock provided the B-Clock Inhibit Switch is ON.

Installation Procedures

DTCU INSTALLATION

The B249 Data Transmission Control Unit (DTCU) may be installed on the "A" or "E" gates of the B452 DFC/DTTU Basic Cabinet or the B450 DFC/DCCU Basic Cabinet. Both of these cabinets contain the necessary Power Supplies and Control functions to properly support a DTCU.

The instructions in this Section apply to installing a DTCU when received, either installed in a Basic Cabinet or, as a Free-Standing Unit.

DTCU RECEIVED AS A FREE-STANDING UNIT

When the B249 DTCU is received as a Free-Standing Unit and is to be installed in a B450 or B452 already on site, observe the following instructions:

1. The physical mounting of the DTCU is performed by first mounting the Maintenance Panel on the desired gate, followed by the Backplane Panel.

2. If the DTCU is mounted in a B452 DFC/DTTU Basic Cabinet, cable the Unit as described in Figure VI-1.

3. If the DTCU is mounted in a B450 DFC/DCCU Basic Cabinet, cable the Unit as described in Figure VI-2.

NOTE

A special Display Control cable is required when the DTCU is installed in a B450 Cabinet.

4. Check for loose or broken wires, proper seating and location of Package, Stick and Cable connection.

DTCU RECEIVED IN BASIC CABINET

When the DTCU is received mounted in either a B450 or B452, observe the following instructions:

1. Check for loose or broken wires.

2. Check all Packages and Sticks for proper location and seating.

3. Tighten all cable Quad connections.

4. Cable DTCU to Terminal Unit(s) as described in Figure VI-1.

SPECIAL INQUIRY TERMINAL CONNECTION

If Inquiry Terminal Units (B481, B483, B484 or B486) are connected to a DTCU, a special cable is required to provide the proper Interface of the Terminal and Control Units. Refer to Note 6 of Figure VI-1 or Note 4 of Figure VI-2.

PLUGGABLE OPTIONS

SCAN COUNTER

If there are less than 15 Terminal Units connected to the DTCU, the Scan Counter logic is arranged to scan only existing Terminals. Remove diodes of Diode Stick (DNC) located at AA C5 L6 as shown in Table VI-1 (refer to D.A. Schematic page 28.00.55.0).

TABLE VI-1

MAXIMUM "S" REGISTER COUNT	REMOVE DIODES OF A A C5 L6 (D N C)			
	D	E	F	H
1	X	X	X	
2	X	X		X
3	X	X		
4	X		X	X
5	X		X	
6	X			X
7	X			
8		X	X	X
9		X	X	
10		X		X
11		X		
12			X	X
13			X	
14				X
15				

B300 SYSTEMS

If the DTCU is connected to a B300 System and Inquiry Terminal Units are connected to the DTCU, insert a (DNC) stick (#72477) at location AA C6 Y1. Refer to D.A. Schematic page 28.00.55.5.

B5500 SYSTEMS

If the DTCU is connected to a B5500 System, remove the AND stick at location AE D5 Y9 from all Model III I/O Channels.

Installation Procedures

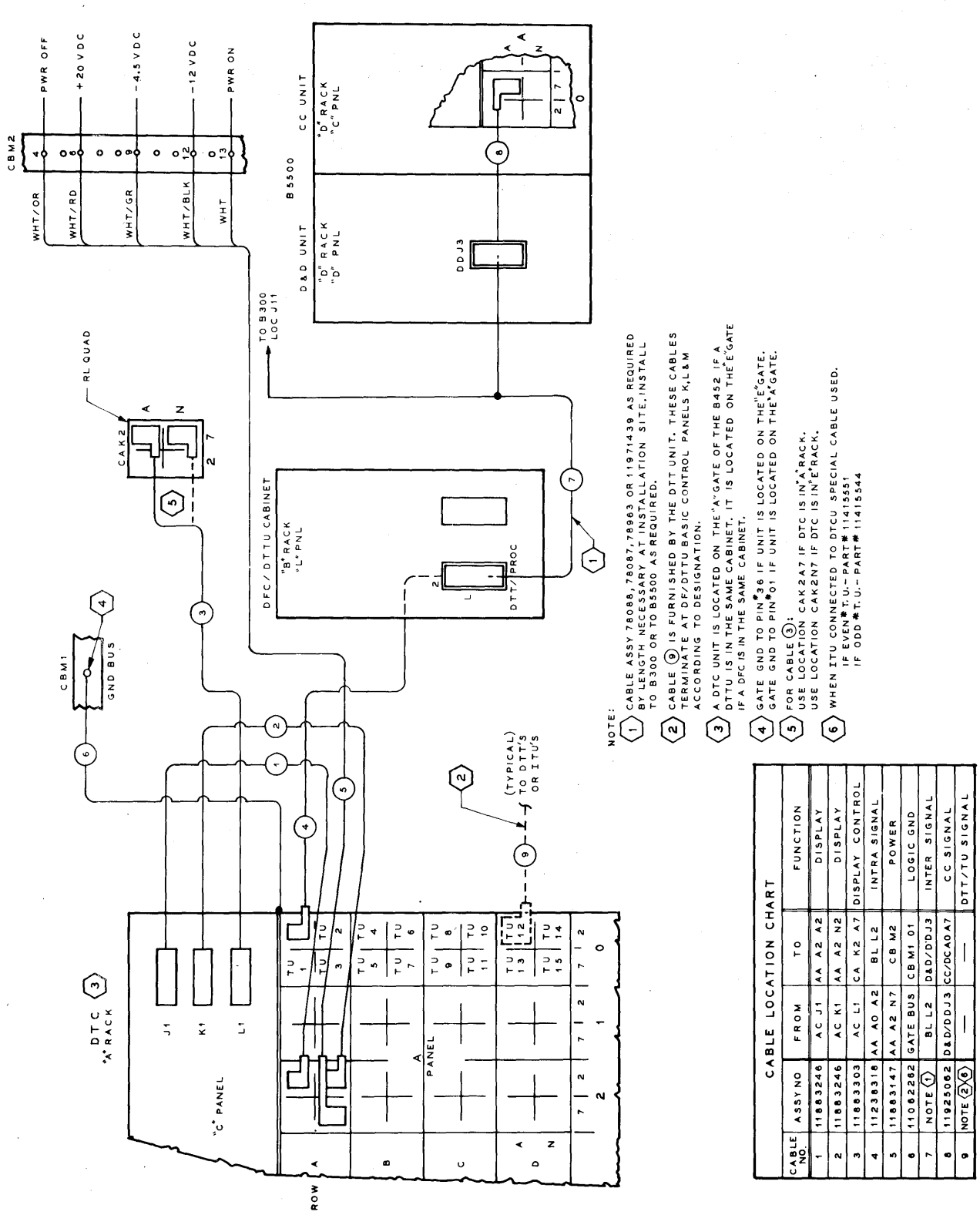
POWER ON

Turn ON the main AC circuit breaker located on the AC control box of the Basic Cabinet. Place the LOCAL/REMOTE switch on the Maintenance Panel in REMOTE. Depress the POWER ON switch; Power should NOT come ON. Put the switch in LOCAL. Again depress the ON switch; Power should come up.

With Power OFF at the System and the DTCU, and the LOCAL/REMOTE switch in REMOTE; depress the Power ON switch at the System. The DTCU Power should also come ON.

SEE PAGES 4 & 5 FOR FIGURES VI-1 & VI-2

Installation Procedures



NOTE:

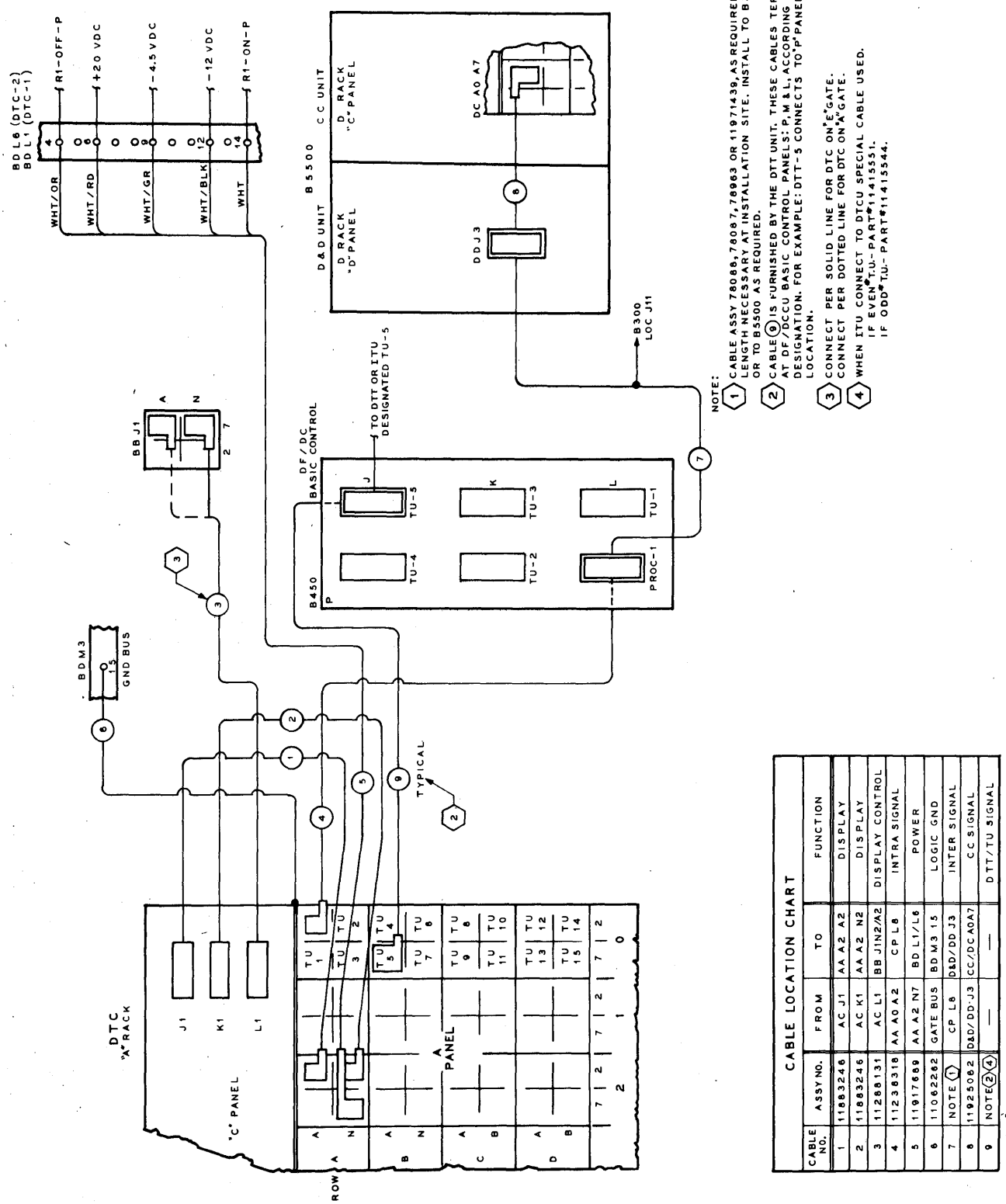
1. CABLE ASSY 78088, 78087, 78063 OR 11971439 AS REQUIRED BY LENGTH NECESSARY AT INSTALLATION SITE. INSTALL TO B300 OR TO B5500 AS REQUIRED.
2. CABLE (9) IS FURNISHED BY THE DTT UNIT. THESE CABLES TERMINATE AT DF/DTTU BASIC CONTROL PANELS K, L & M ACCORDING TO DESIGNATION.
3. A DTC UNIT IS LOCATED ON THE "A" GATE OF THE B452 IF A DTTU IS IN THE SAME CABINET. IT IS LOCATED ON THE "E" GATE IF A DFC IS IN THE SAME CABINET.
4. GATE GND TO PIN #36 IF UNIT IS LOCATED ON THE "E" GATE. GATE GND TO PIN #01 IF UNIT IS LOCATED ON THE "A" GATE.
5. FOR CABLE (3): USE LOCATION CAK2A7 IF DTC IS IN "A" RACK. USE LOCATION CAK2N7 IF DTC IS IN "E" RACK.
6. WHEN ITU CONNECTED TO DTCU SPECIAL CABLE USED. IF EVEN # T.U. - PART # 11415551 IF ODD # T.U. - PART # 11415544

CABLE LOCATION CHART

CABLE NO.	ASSY NO	FROM	TO	FUNCTION
1	11883246	AC J1	AA A2 A2	DISPLAY
2	11883246	AC K1	AA A2 N2	DISPLAY
3	11883303	AC L1	CA K2 A7	DISPLAY CONTROL
4	11238316	AA A0 A2	BL L2	INTRA SIGNAL
5	11883147	AA A2 N7	CB M2	POWER
6	11062282	GATE BUS	CB M1 01	LOGIC GND
7	NOTE (1)	BL L2	D&D/DDJ3	INTER SIGNAL
8	11925062	D&D/DDJ3	CC/DCA0A7	CC SIGNAL
9	NOTE (2)(6)	—	—	DTT/TU SIGNAL

FIGURE VI-1
DTCU MOUNTED IN B452

Installation Procedures



CABLE LOCATION CHART

CABLE NO.	ASSY NO.	FROM	TO	FUNCTION
1	11883246	AC J1	AA A2 A2	DISPLAY
2	11883246	AC K1	AA A2 N2	DISPLAY
3	11288131	AC L1	BB J1N2/A2	DISPLAY CONTROL
4	11238318	AA A0 A2	CP L8	INTRA SIGNAL
5	11917659	AA A2 N7	BD L1/L6	POWER
6	11062262	GATE BUS	BD M3 15	LOGIC GND
7	NOTE (1)	CP L8	D&D/DD J3	INTER SIGNAL
8	11925062	D&D/DD-J3	CC/DC A0A7	CC SIGNAL
9	NOTE (2)(4)	—	—	DTT/TU SIGNAL

FIGURE VI-2
DTCU MOUNTED IN B450

Installed 5/20/75 JH

Burroughs FIELD ENGINEERING TECHNICAL OPERATIONS	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B300/B5500	No. 6259-006
		STYLE/MODEL B249	PAGE 1 OF 1
		TOP UNIT NO. 1121 0440	
STD. INSTALL. TIME Up to 1/2 hour	UNITS AFFECTED ALL	UNIT DESCRIPTION Data Trans. Control	
TITLE Prevent System Interrupt with DTCU in Local EI 30706			DATE 5-11-72

PREREQUISITE: None

PURPOSE:
To eliminate interrupts being sent to the system when DTCU is in local.

PARTS REQUIRED: None

INSTRUCTIONS: Add the following wire:

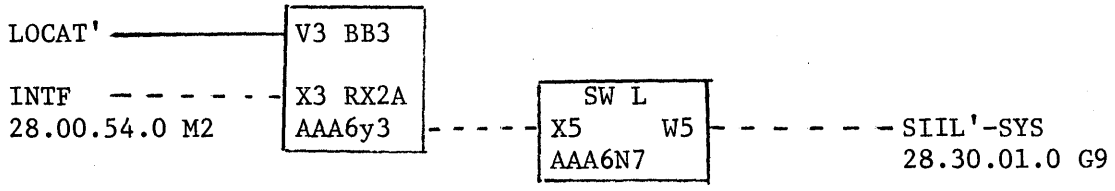
Ckt. No.

2830200K16 Add AAA6B4 Z2 to AAA6V3 Z2

Redline logic book as follows:

SIIS'-SY SWL
-O'- SIIL'-Sys$SET INQUIRY INTERRUPT-Not to System$
-I- INTF' LOCAT'1 *USE 'B' STICK
ADD

Redline schematic page 28.00.23.0 as follows:



This is in JH 5/20/75

Burroughs FIELD ENGINEERING TECHNICAL OPERATIONS	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B300/5500	No. 6259-005 REVISED
		STYLE/MODEL B249	PAGE 1 OF 2
		TOP UNIT NO. 1121 0440	
STD. INSTALL. TIME Up to 1 Hour	UNITS AFFECTED All	UNIT DESCRIPTION Data Transmission Control	
TITLE PROVIDE SEPARATE BIAS PACKAGE FOR EACH CLOCK		EI 30619	DATE 6-9-72

PURPOSE: To eliminate interaction of the clocks due to feedback on the bias circuit. (The feedback has been found to cause many previously unexplained problems.)

PARTS REQUIRED:

Part No.	Description	Qty.	Unit List Price
✓ 1178 4287	PI-Variable Bias	1	$69.00

INSTRUCTIONS:
Perform the following backplane wiring changes:

Delete circuits:

Ckt No.	From	El. Type	Z	To	El. Type	Z
2800320C33	AAC8U0	FSB	2	AAC8K2	VB	2
2840045G55	AAD5E3	SW H	2	AAD6E3	FSB	2

Add circuits:

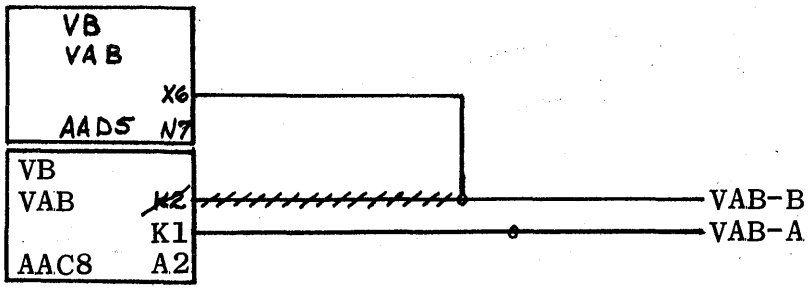
2800320C33	AAC8U0	FSB	2	AAD5X6	VB	2
2840045G55	AAD5P7	VB	1	AAD6E3	FSB	2
2840045G55	AAD5E3	SW H	2	AAD5P7	VB	2
2840000B75	AAD5U7	VB	1	AAC5Z6		1
2840000B85	AAD5V7	VB	1	AAC5Z7		1

✓Install 1178 4287 PI-Variable Bias package at location AAD5N7.

DOCUMENT UPDATE:
Redline Circuit List 1121 6793 and Module Locator 1121 6801 using the preceding information.

Redline Logic Book 1122 4201 as shown on page 2 of this RIN.

Redline DTC DA Schematic Page 28-00-32-0 as follows:



✓Changes or additions since last issue

Schematic Page 28.00.32.0

CLP-A CLNQ

-Ø- A-CLOCK $A-CLOCK CLOCK PULSE$

-IV1- * DO NOT CONNECT *

-IV2- * DIRECT INPUT FROM 02 OF VB * ← Delete

VB * ← Add

CLP-B CLNQ

-Ø- B-CLOCK $B-CLOCK CLOCK PULSE$

-IV1- * DO NOT CONNECT *

-IV2- * DIRECT INPUT FROM 01 OF VB * ← Delete

VB * ← Add

VABV VB

-01- * TO DIRECT INPUT IV2 OF CLP-B CLNQ * ← Delete

-02- * TO DIRECT INPUT IV2 OF CLP-A CLNQ *

-Ø-

← Add ← Delete

VABV VB

-Ø- * TO DIRECT INPUT IV2 OF CLP-B CLNQ * ← Add